Master's Thesis

Measurement and Analysis of Electromagnetic Field, Noise and IC Logic Error due to system-level ESD

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2017

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A thesis

submitted to the Graduate School of UNIST

in partial fulfillment of the

requirements for the degree of

Master of Science

Myungjoon Park

06. 30. 2017

Approved by

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Advisor

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06. 30. 2017

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Abstract

As the high performance very-large-scale integration (VLSI) systems operate with high speed and low voltage, the system-level electrostatic discharge (ESD) event is becoming one of the important noise sources causing logic errors and system malfunctions such as system reboot or fault. To understand the ESD noise phenomena and improve the system-level ESD noise immunity for devices, the accurate ESD noise measurement and analysis of IC logic errors are necessary.

Section I is written for the tendency of ESD research and previous research. This paper presents the noise type correlation by measuring the signal-ground noise and power-ground noise simultaneously on the fundamental F/F operation circuit and shows the type of error from chip, in section II. Furthermore, the decoupling capacitors (de-cap) effect that can reduce the error occurrence by checking the error rate are analyzed. A generator is designed on the main board which is based on real operating laptop, and the chip on dual in-line memory module (DIMM) is also designed to perform the basic F/F operation. The clock and data input from generator are connected to the chip on the DIMM through the small outline dual in-line memory module (SODIMM) socket. ESD occurs at the corner of the ground plane of main board. The specification of the ESD generator satisfies IEC 61000-4-2 [1]. The ESD current flows along the ground strap, and affects the DIMM. IN-ground, CLK-ground, OUT-ground and power-ground on the DIMM are simultaneously measured to determine the effect of ESD on the main board. To analyze the error ratio according to the ESD voltage level, the voltage setup of the ESD gun is 3kV, 5kV and 8kV. To investigate the effects of chip shielding and DIMM de-caps on the error probability of DIMM, the experiment is conducted under the several conditions. After confirming the normal operation for each condition, the error type on the DIMM due to the ESD occurred in the circuit is analyzed and the statistics are shown. The results are verified by H-spice simulation, Vector Network Analyzer (VNA) and HFSS simulation. In order to obtain the improvement method of the DIMM immunity, experiments are conducted to find out the effective position and number of DIMM de-cap.

Accurate measurements of electromagnetic fields are also essential to analyze the radiated noise due to unwanted electrostatic discharge (ESD) events at electronic devices. Usually, to know the radiated noise by ESD events, the voltages induced at field probes are measured, and the fields are obtained from the voltage by de-convolving the probe factor. In section III, the two probe-factor deconvolution methods are investigated and compared in the measurements of the fields induced by system-level ESD events.

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I. Introduction

1.1 Research Background

1.1.1 Electrostatic discharge (ESD)

Electrostatic discharge (ESD) is one of the most common EMC problem and is becoming a major cause of malfunction in various electronic devices such as notebooks and smart phones since the ESD event contains high voltage and high current with fast rise time, as depicted in Figure 1. ESD is defined as “the sudden flow of electricity between two electrically charged objects caused by contact”.

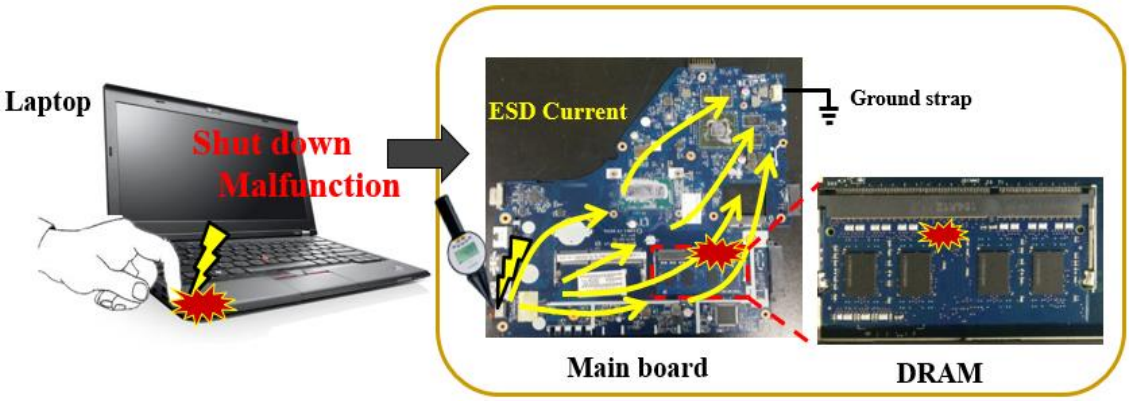


Fig. 1. System-level ESD due to an ESD event

1.1.2 Trend of ESD research and Motivation

The effects of ESD on integrated circuits (ICs) and Electronic devices can be broadly categorized as follows. The first is chip-level ESD that occurs during IC fabrication or assembly and causes physical damage to the IC. The second is system-level ESD that occurs during the operation of the finished system and causes malfunction. Countermeasures of the hard failures have been actively pursued by semiconductor process and circuit researchers for a long period of time because hard errors cause permanent damage due to physical destruction of the IC. However, since the soft error is an unexpected malfunction during the operation of the completed system, the mechanism or phenomenon of system-level ESD is distinct from that of chip-level ESD and the solutions are different. Recently as the number of mobile and wearable devices has increased, contact between electronic devices and people has become frequent. Therefore, the probability of malfunctions is rapidly increasing, and precise analysis and countermeasures for system-level ESD are required. Soft failure due to ESD is divided into conducted noise coupling and direct coupling to wire-bond and IC die. For precise

analysis of the soft error, the accurate measurement method is given priority. In the case of conduction noise, the transient noise measurement on a decoupling capacitor using the oscilloscope and the Z parameter measurement techniques are developed [2]-[4]. In case of direct coupling to wire-bond and IC die, measurement technique using field sensors or method of converting the measured voltage values into field quantities using a field probe was proposed [5]-[9]. Simulation and modeling techniques were studied to verify these measurement methods [5] and numerical analysis methods using partial element equivalent circuit (PEEC) were developed to facilitate calculation and analysis of system-level ESD [10], [11]. And the relation between of ESD field coupling and metal chassis or printed circuit board (PCB) ground was investigated [12]. However, these studies focus on the noise analysis rather than analysis of operation error phenomenon caused by ESD. In order to analyze the malfunction phenomenon and ask for countermeasures, it is necessary to analyze the normal operation according to ESD occurrence in the circuit as well as noise analysis. Recently, studies have been conducted to understand the soft error of digital IC by modeling a simple D flip-flop (F/F) or suggesting a delay model and prediction for generic logic circuit that can occur during electromagnetic disturbances [13], [14], and [15] states the improvement method of system-level ESD reproducibility.

1.2 Previous Research

There have been several studies related to the system-level ESD. In 2003, Kai Wang has proposed and validated the numerical modeling of the electrostatic discharge generator. The discharge current and transient fields of an ESD generator are numerically simulated, as shown in Fig. 2.

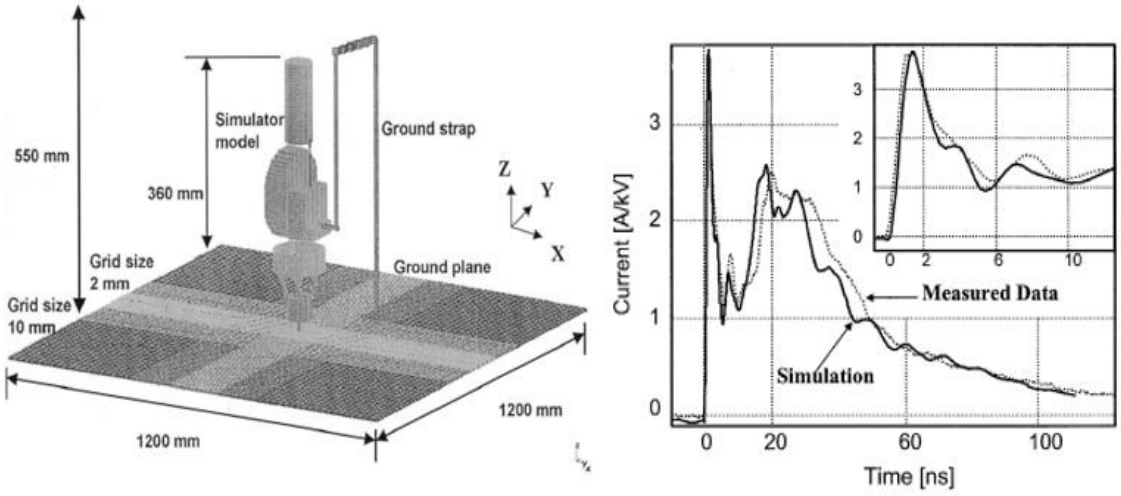
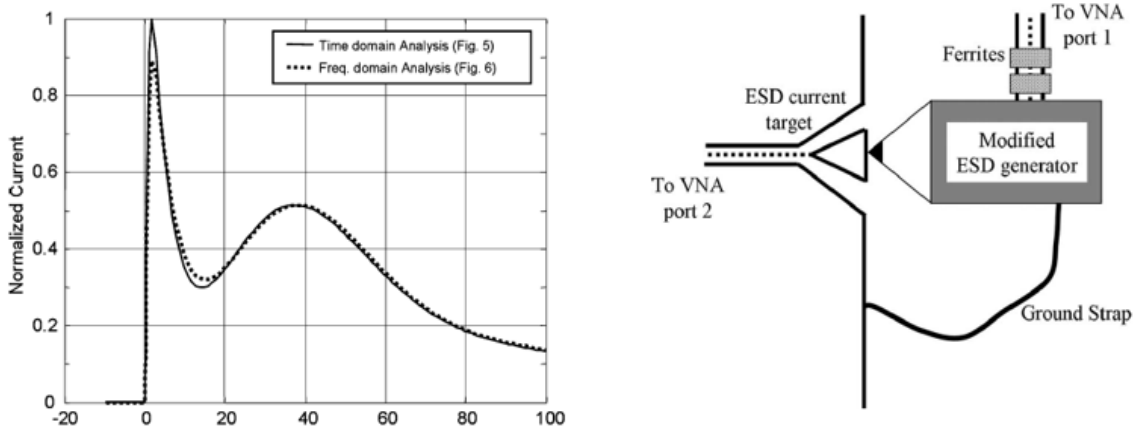


Fig. 2. Model of the short-ground strap (80-cm-long) domain and comparison of simulated and measured discharge currents

In 2007, Jayong Koo have analyzed the ESD measurement method using the frequency domain measurement technique. Fig 3 shows the comparison of computed currents using time domain and the frequency domain and schematic of frequency-domain measurement setup using Vector Network Analyzer(VNA).



(a) (b)

Fig. 3. (a) Comparison of computed currents using time-domain and frequency domain analysis (b) Frequency-domain measurement setup using VNA for the discharge current waveform

In 2015, Guangyao Shen have conducted the soft error of digital IC by modeling a simple D flip-flop as shown in Fig 4.

Table 1 denotes the previous research to work this research.

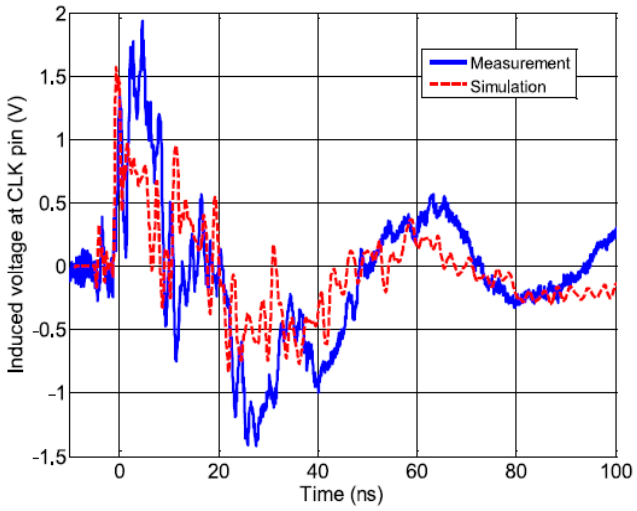


Fig. 4. (a) Comparison between measured and simulated input (IC clock) wave forms when ESD occurred.

Table 1

PREVIOUS RESEARCH

Title	Numerical Modeling of Electrostatic Discharge Generators	Frequency-domain measurement method for the analysis of ESD generators and coupling	ESD Immunity Prediction of D Flip-Flop in the ISO 10605 Standard Using a Behavioral Modeling Methodology	**This work**
Authors	Kai Wang	Jayong Koo	Guangyao Shen	**Myungjoon Park**
Publish (Year)	IEEE Trans. on EMC (2003)	IEEE Trans. Electromagnetic. Compat. (2007)	IEEE Trans on Electromagnetic. Compat. (2015)	**A master's thesis (2017)**
Main contribution	The current and fields from an ESD simulator using the geometry and the charge voltage are obtained and validated	A frequency-domain method for conducting coupling studies associated with ESD generator	An alternative modeling method is proposed, which emphasized ease of IC characterization and model implementation	**Measurement and Validation of Noise and IC logic error due to system-level ESD**

II. Analysis and Validation of IC Soft Errors due to System-Level ESD noise

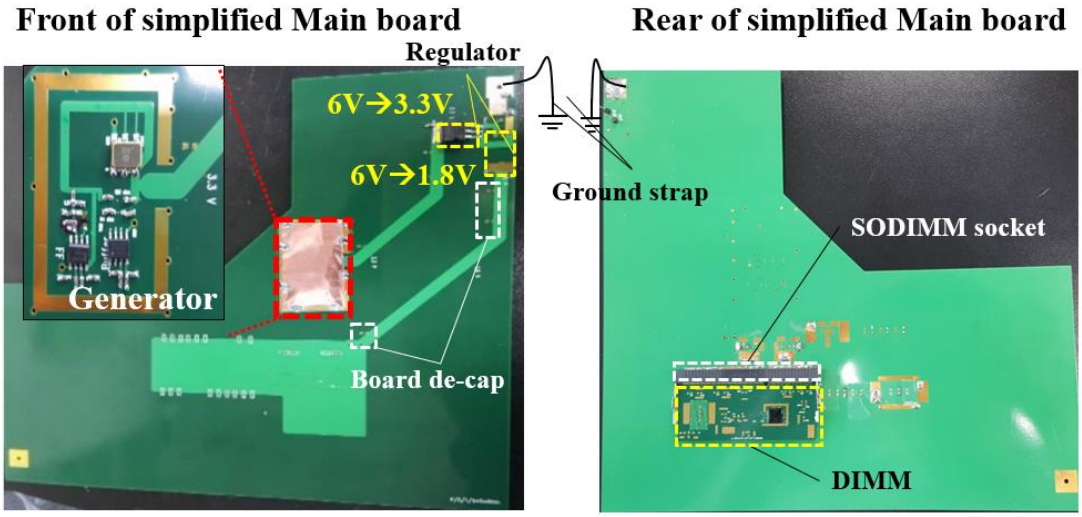
2.1 Simplified PCB Structure for System-Level ESD Noise Analysis

2.1.1 The Simplified Mainboard Description

Mainboard consists of 4 layers, as shown in Fig. 5 (a). Each layer is made of copper with a thickness of 0.035mm and the size of the PCB is 220×230mm. The first layer represents the power plane, second and fourth layers are ground plane and the signal trace goes through the third layer. The thickness between each plane is 0.3mm, 0.1mm and 0.1mm and is filled with dielectric material FR-4. Signal traces widths are set to 0.167mm through the transmission line impedance matching. The ground plane of PCB is connected to an aluminum plane on the floor by a ground strap. The power supply is used to provide 6V to the main board. It is converted to 3.3V and 1.8V through two regulators and supplied to generator and power plane, respectively. 3 capacitors of 10uF are connected for stable DC supply to the generator and power plane. As depicted in Fig. 5 (b), the generator consists of the voltage controlled crystal oscillator with 200MHz, D-type F/F and clock buffer. IN is obtained from F/F and CLK is obtained from clock buffer. These signal lines are place on the third layer and are connected to the chip of DIMM through the SODIMM socket. According to the specification of the crystal oscillator, frequency swing of CLK is 200MHz. Meanwhile, the frequency of IN is 100MHz, because IN changes from low to high or high to low at the rising time of the CLK. The source terminations of IN and CLK are connected to ground at 100 Ω and 50 Ω SMT resistors are connected between the signal from generator and chip on DIMM, between chip on DIMM and ground.

If an ESD occurs at the left corner of PCB, an unexpected error from generator can occur due to field coupling in the generator. In fact, when the generator is not protected completely, the phase

inversion error of the output from chip on DIMM is occurred due to malfunction of mainboard generator.



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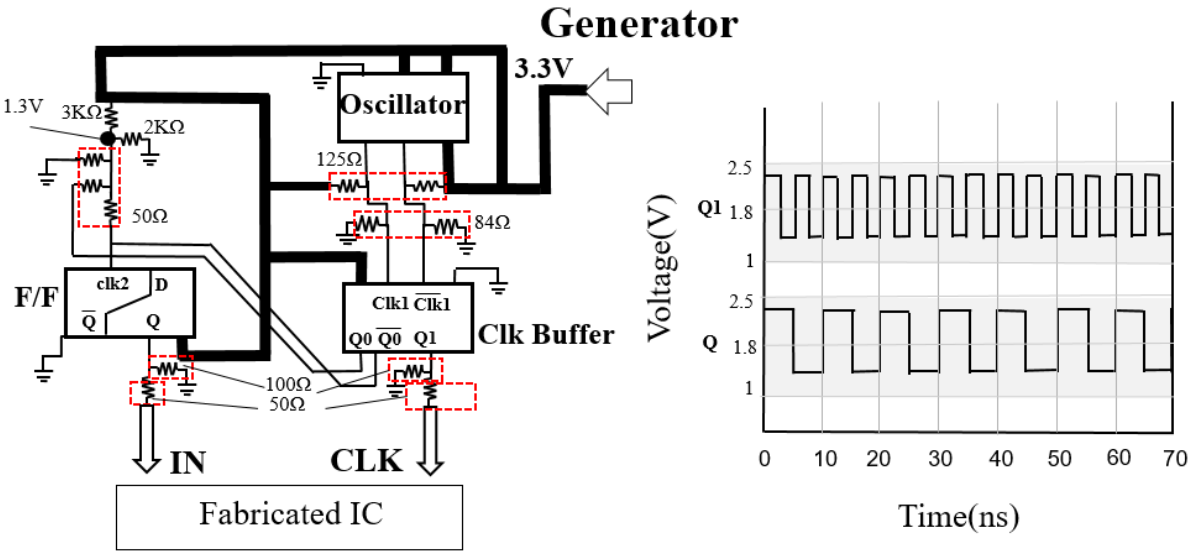
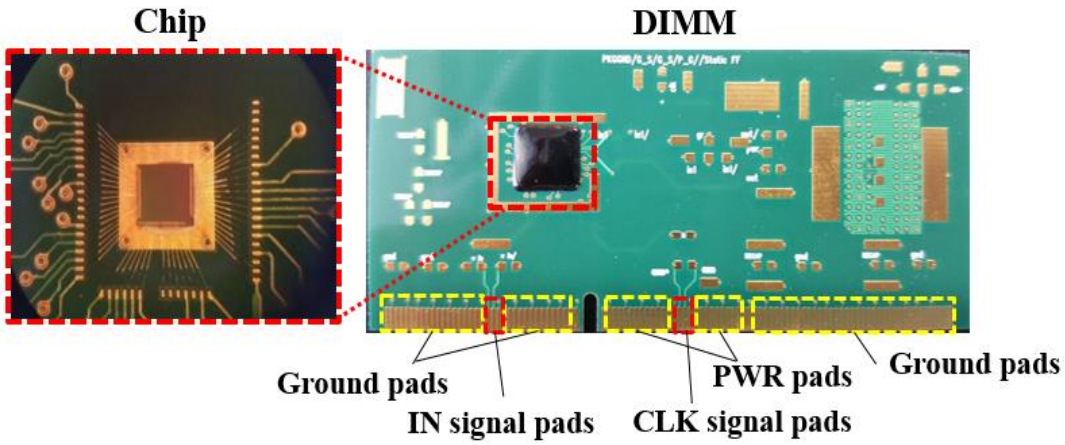


(b)

Fig. 5. (a) Simplified mainboard (b) Schematic of simplified mainboard circuit

2.1.2 The Chip on Board(COB) Structured DIMM Description



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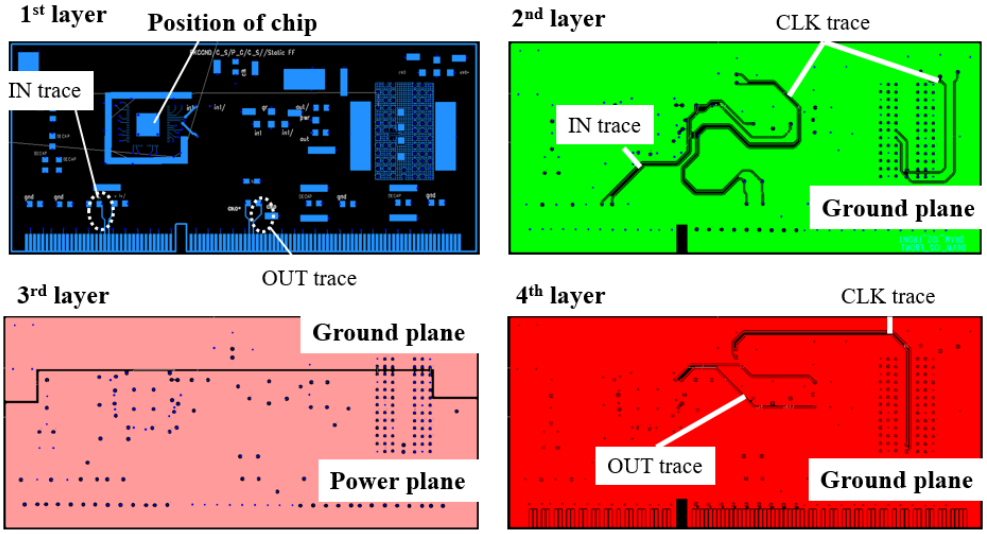

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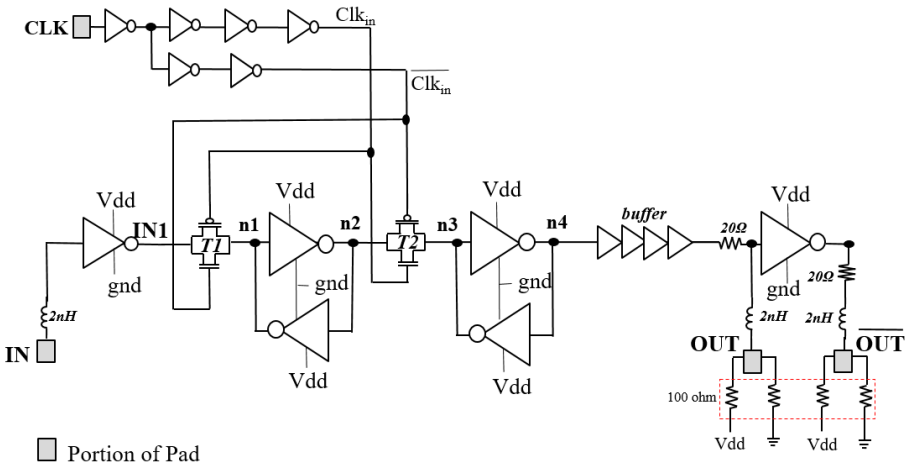

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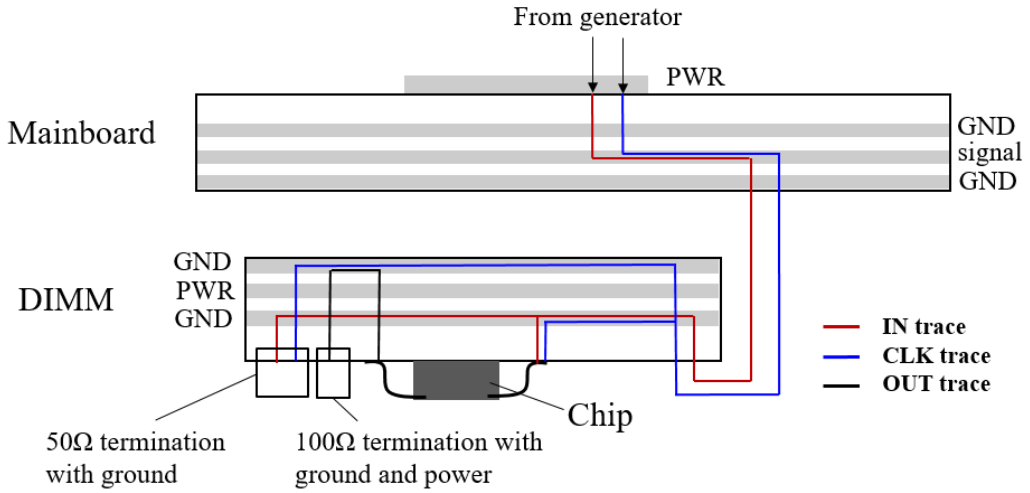


(d)

Fig. 6. (a) Photograph of DIMM (b) PADS layout (c) Static F/F circuit (d) Layout of signal trace

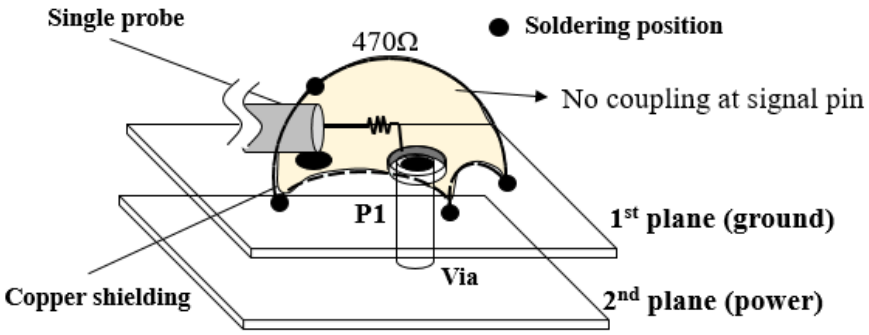
IN and CLK signals started from the generator of the mainboard are passed to the first layer of COB structured DIMM through the SODIMM socket as shown in Fig. 6 (a). The DIMM consists of four 68mm×30mm layers and the gap between each copper layer is 0.3mm, 0.1mm and 0.1mm and is composed of FR-4. As shown in Fig. 6 (b), the first layer is the area where the ground of lab-made chip is connected, second and fourth layers are comprised of the ground plane and signal trace, and the third layer has power plane and ground plane. The fourth layer of DIMM faces the fourth layer of mainboard. The total number of pads of the first and fourth layers are 204 and pin assignment follows the data sheet of double data rate 3 synchronous DIMM SODIMM (DDR3L SDIMM SODIMM). The 52 pads located at both end of the DIMM concatenates between ground plane of mainboard and that of DIMM module. The 18 pads located at the center of the DIMM connect the power planes. The CLK signal, which has passed through first layer of the DIMM, flows into the chip from the second layer through the via. And it is terminated with 50 Ω after passing through the fourth layer. IN is connected to the chip at the second layer through the via and terminates with 50 Ω at the corner of the DIMM. Fig. 6 (c) shows the static F/F used for measurement. Half swing CLK changes to full swing Clk_{in} and $\overline{Clk_{in}}$ after passing the clock buffer at chip. Clk_{in} and $\overline{Clk_{in}}$ operate the transmission gate, transmission gate 1 (T1) passes IN1 when CLK is falling time and when the Clk_{in} is rising time, transmission gate 2 (T2) passes n2. Finally, OUT is the result of passing through the data store inverter and buffer from n3, $\overline{OUT}$ is the inversion state of OUT. The termination resistance with ground plane or power plane of OUT and $\overline{OUT}$ are 100 Ω. Fig. 6 (d) shows the layout of signal trace.

The IN trace does not cross the power plane at DIMM. On the other hand, the CLK trace and OUT trace pass through the power plane through the vias.

2.2 Measurements Using Oscilloscope and VNA

2.2.1 Noise Voltage Measurement Method Using the Rigid Cable

Since the ESD gun is shielded and the distant from the measurement probes, the direct effect from the gun body to the probes is assumed to be negligible. Fig. 7 shows the measurement setup for power-ground noise induced by ESD event. The outer and inner conductors of a semi-rigid cable are connected to power plane and ground plane. In the several kilovolt ESD event, the ground plane in the PCB can fluctuate up to a few hundreds or thousands voltage with reference to the ideal zero potential. The strong common-mode (CM) noise voltage is also captured in the instruments, which makes the accurate measurement of the differential power-ground noises very difficult.



$$V_{measure} = V_{real} \times \frac{50}{520}$$

Fig. 7. Measurement method of the Power-Ground Voltage Fluctuation.

Ferrite cores are commonly installed at a measurement cable to reduce the CM noise. A number of ferrite cores are also installed along the probe-oscilloscope connection cable in all the measurements. After great reduction of the strong common-mode noises using many ferrite cores, the relatively small power-ground fluctuation in the differential mode (DM) can be measured in the oscilloscope.

However, there is another obstacle for accurate measurement of power-ground noise. While the electric field coupling at the ground of probe is prevented using the ferrite cores, the strong electric field can be still directly coupled to the signal pin of rigid cable. Hence, the signal pin was covered with a piece of copper tape in the measurement. The copper tape is soldered to the ground of the rigid cable and the ground plane of the PCB at several positions, which makes the potential of copper tape

and the PCB ground plane electrically same removing electric field inside the copper tape. This setup requires a careful attention so that the signal pin of the probe does not adhere to copper tape. With applying the aforementioned two techniques, the differential-mode power-ground fluctuation can be accurately measured. Also, to make the high impedance probe, a 470 Ω SMT resistor is connected in series at the signal pin of rigid cable. With the cable characteristic impedance of 50Ω, the total input impedance is 520ohm, resulting that the measured voltage is about a tenth of the real one. ($V_{meas}=V_{real} \times 50/520$)

2.2.2 PCB Measurement Using the Oscilloscope

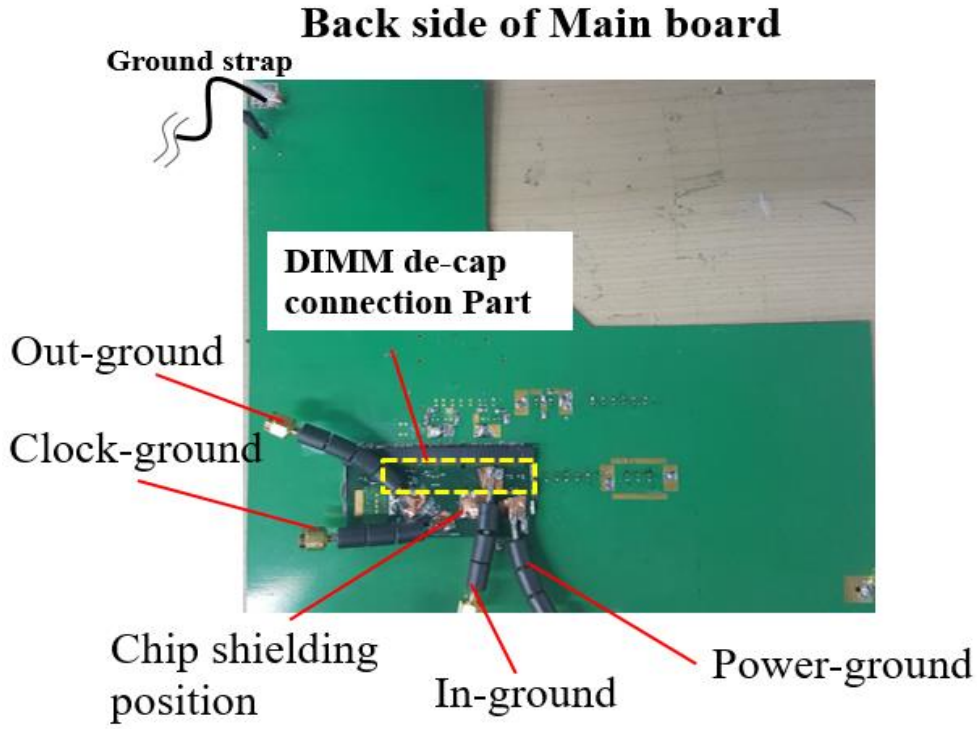


Fig. 8. Measurement position of signal-ground noise and power-ground noise

Experiments are conducted to measure the noise voltage between the power plane and the ground plane, the noise voltage between signals and ground plane under the 3kV, 5kV and 8kV ESD occurrence conditions. The correlation between each noise is analyzed by measuring the Power-ground noise, CLK-ground noise, IN-ground noise and OUT-ground noise simultaneously using the 4 channels of the oscilloscope. The experimental conditions are dependent on the w/ or w/o of chip copper shielding, w/ or w/o of DIMM de-caps, as shown in Table I. All of the capacities of de-caps are 10uF and the experiments is carried out 50 times in each case. The location of the DIMM de-caps are shown in Fig. 8. Even in the case of the same signal trace, there are exist difference of delay and noise peak depending on the measurement position. Since the main purpose of the experiment is to observe chip error on DIMM, measurements are taken to meet both the nearest points at the chip and

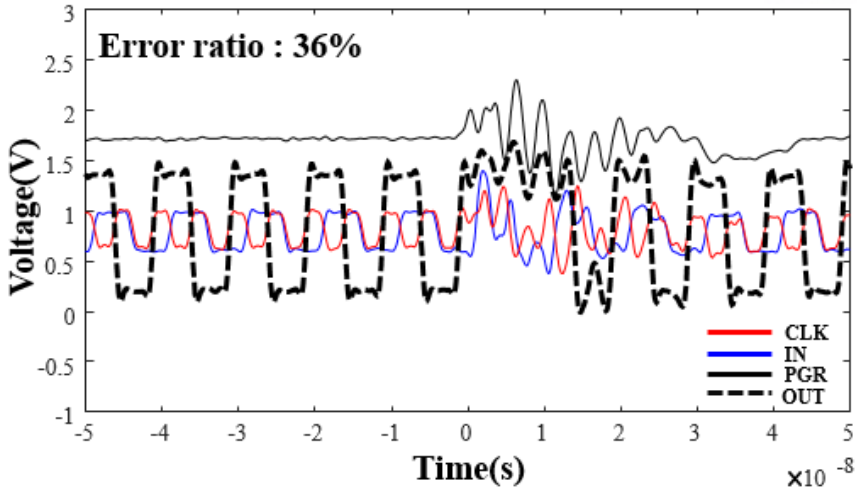
physically measurable points on DIMM. The single probe used in the measurement is rigid cable filled with ferrite cores. The outer ground of rigid cable is connected to ground plane of DIMM and signal pin with 470Ω SMT resistor is connected to signal trace or power plane.

The error from chip in the experiment is defined as the non-normal temporary High/Low of OUT-ground noise. Fig. 9. shows some of the experimental results depending on the three measurement conditions when the ESD occurrence voltage is 5kV. The case of chip shielding and Board de-cap×3 is default condition. As can be seen from the measurement results, because the signal traces pass through the power plane or the ground plane and cannot avoid the influence of the field coupling between these two planes due to ESD, all the signal-ground noises follow the form of power-ground noise. Comparing the measurement results w/ or w/o chip shielding, the noise is not significantly different. But the error rate of chip shielding case (26%) is less than the no chip shielding case (36%). It is considered that the error ratio is reduced by blocking the direct coupling to wire-bond and IC die that connects the chip and DIMM through the chip copper shielding.

Table 2

MEASUREMENT AND SIMULATION CONDITIONS

	Case0	Case1	Case2
Chip shielding	**X**	**O**	**O**
Board de-cap	**3**	**3**	**3**
DIMM de-cap	**0**	**0**	**5**



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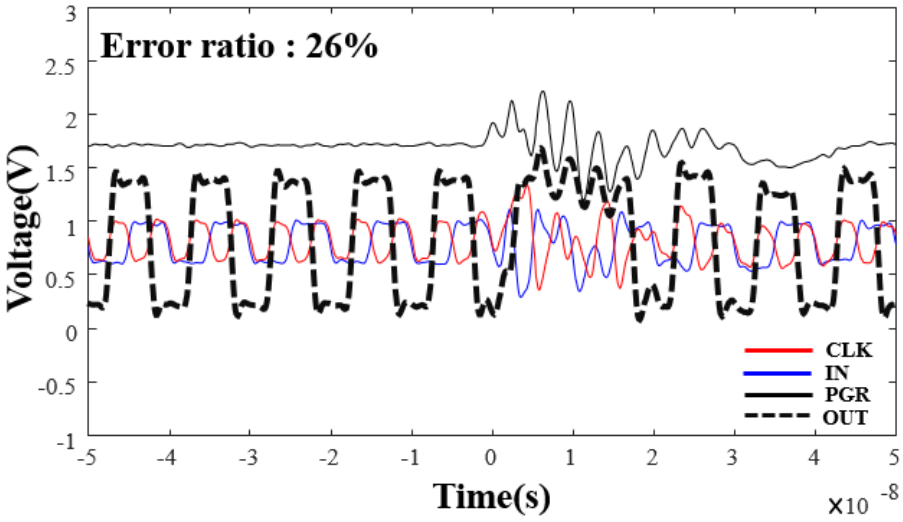

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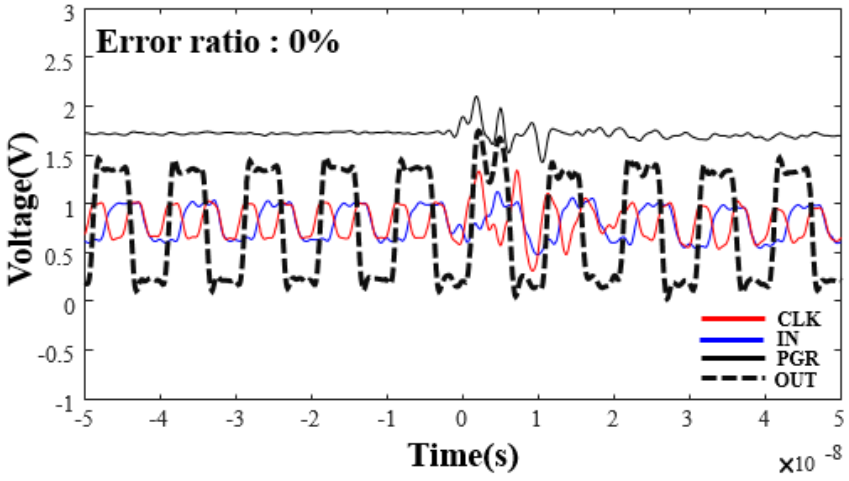
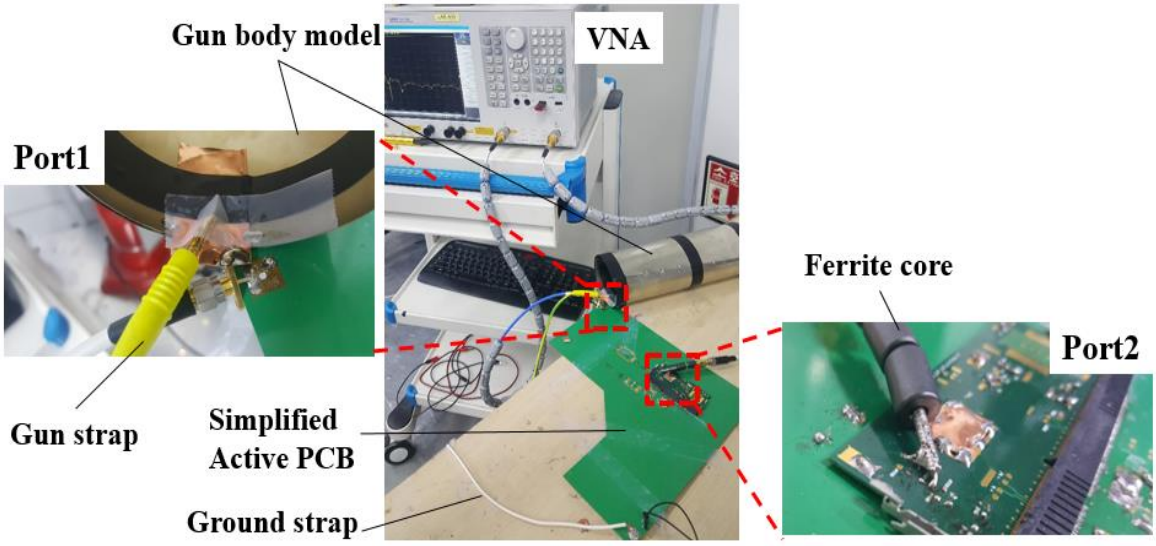


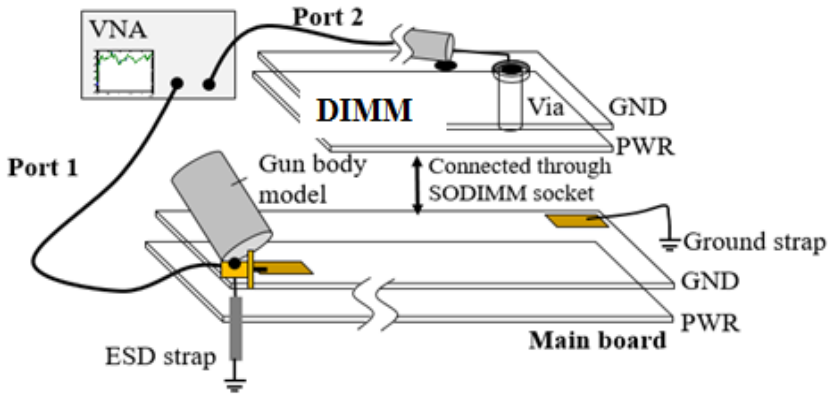
(c)

Fig. 9. Noise voltage measurement results at 5kV ESD occurrence and error ratio obtained from 50 times measurements (a) Error case: case0 (b) Error case: case1 (c) No error case: case2

2.2.3 Validation Using the Z_{21} Measurement Technique and HFSS Simulation



(a)



(b)

Fig. 10. (a) Photograph of Z_{21} measurement set-up (b) Schematic of port conditions

At first, the measured results of power-ground noise voltage on DIMM are verified by multiplying input current and Z parameter using Vector Network Analyzer (VNA) [2]-[4]. Input current is measured by connecting the current probe CT1 to the ground of mainboard while 5kV ESD occurrence. As shown in Fig. 10 (a), the RF measurement cable is used for connecting with Port1 and Port2. Each Port1 and Port 2 is composed of SMA port and lab-made single probe to connect with RF measurement cable. Both RF cables and the single probe are filled with ferrite cores to remove the

common mode noise effectively. Fig. 10 (b) shows the schematic of port connections. The signal pin of Port1 is connected to the position of ESD occurrence on the main board, and the Port1 ground is connected to the gun body model to take self-capacitance of ESD gun into consideration. The gun body model is an aluminum cylindrical shape similar to the actual gun size. Meanwhile, the signal pin of Port2 single probe is connected to the power plane on the DIMM, the ground plane and the outer ground of Port2 single probe are soldered. Although the signal pin of Port1 and the outer metal of Port2 are the same ground, there is no problem with the measurement because the distance between the Port1 of mainboard ground and Port2 of DIMM ground is far enough.

For additional comparison between measurement and simulation, the structure of mainboard and DIMM is also simulated in a full wave solver, Ansys HFSS, as shown in Fig. 11. In the simulation model, the size of ESD gun body and PCB are same with the real structure. Port1 connects the gun strap with SMA signal pin which is connected with ground pad of main board. The position of port2 is same with the power-ground measurement position. To consider the pad inductance, pad L is connected in series with port2. The main board is connected to the DIMM by a SODIMM socket which is made of copper. For efficient analysis of the measured results, the equivalent circuit was modeled and the measurement and simulation Z_{22} and Z_{21} are plotted in Fig. 12. The Z_{21} of the case1 and the case2 in HFSS simulation and measurement using the VNA are shown in Fig. 12 (a). In case of default, 2 peaks at Z_{22} can be found as shown in Fig. 12 (b). The total parasitic inductances and parasitic resistances of the board de-caps at main board power line (L_{d1} and R_{d1}) are 0.2nH and 300mΩ. The total capacitance of de-caps (C_{d1}) is 25uF. The R, L and C parameter of chip (R_{chip}, L_{chip} and C_{chip}) is set to 0.3nH, 60mΩ and 3000pF, separately. The first peak is the resonance between the mutual capacitance of power plane and ground plane at DIMM (C_{DIMM}), C_{chip}, L_{chip}, L_{d1}, power socket inductance (L_{pwr}) and ground socket inductance(L_{gnd}) and the value is about 50MHz. Peak2 is influenced by capacitance between power plane and ground plane at main board (C_{board}), L_{gnd}, L_{pwr} and L_{chip}. The resonance of peak2 is about 300MHz. When the de-caps are connected to the DIMM as shown in Fig. 12 (c), the resonance frequency of first peak is increased by the parasitic inductance (ESL) value of the DIMM de-cap and magnitude of Z_{21} is decreased by the ESR. The frequency of the second peak is also affected by ESL and ESR of the DIMM de-cap, and the Z_{22} appears as peak3. The capacitance, parasitic resistance (ESR) and ESL of total DIMM de-caps (C_{d2}, R_{d2} and L_{d2}) is 42.1uF, 180mΩ, 0.22nH each. The peak point of Z_{21} corresponds to the peak point of Z_{22}. Table II shows the component values in the equivalent circuit. The ESL, ESR and the capacitance of de-cap is measured by the shunt-through technique used for low impedance passive electronic component. The mutual capacitances of main board and DIMM, self capacitances of main board ground plane, power plane and self capacitance of DIMM power plane are extracted using the commercial solver, Ansys Q3D.

The calculation results and simulation results in time domain for the case1 and case2 are compared with the oscilloscope measurement results, as shown in Fig. 13. Similar results can be seen in four

cases.

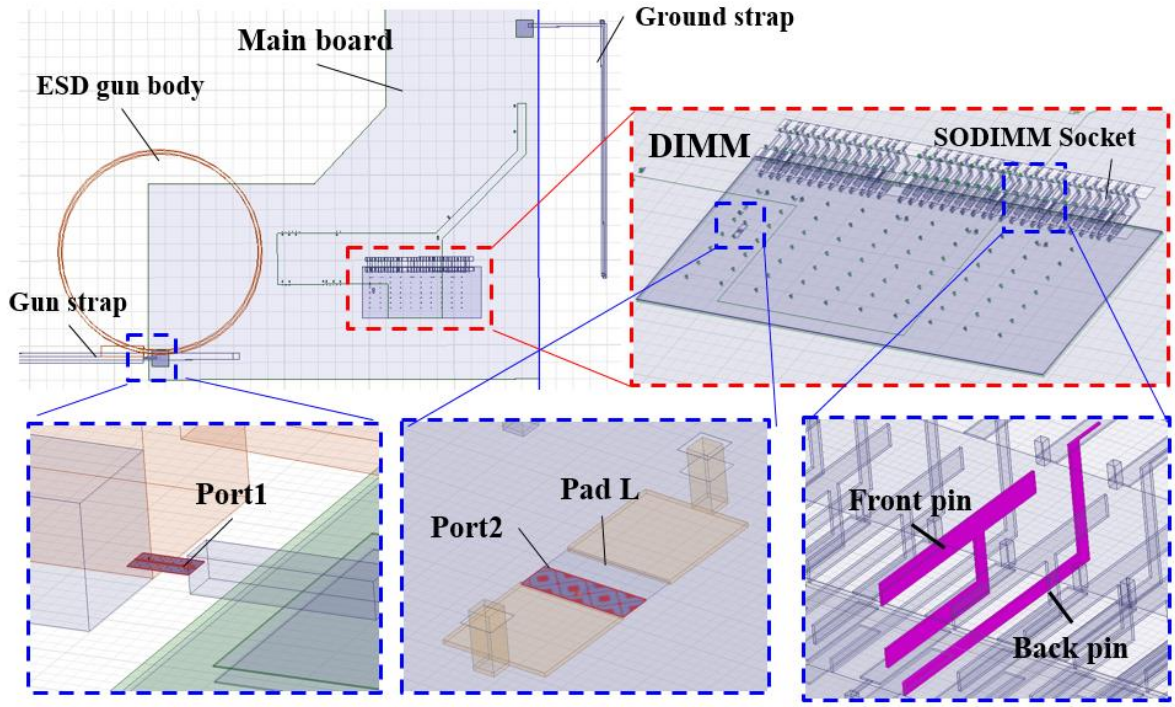
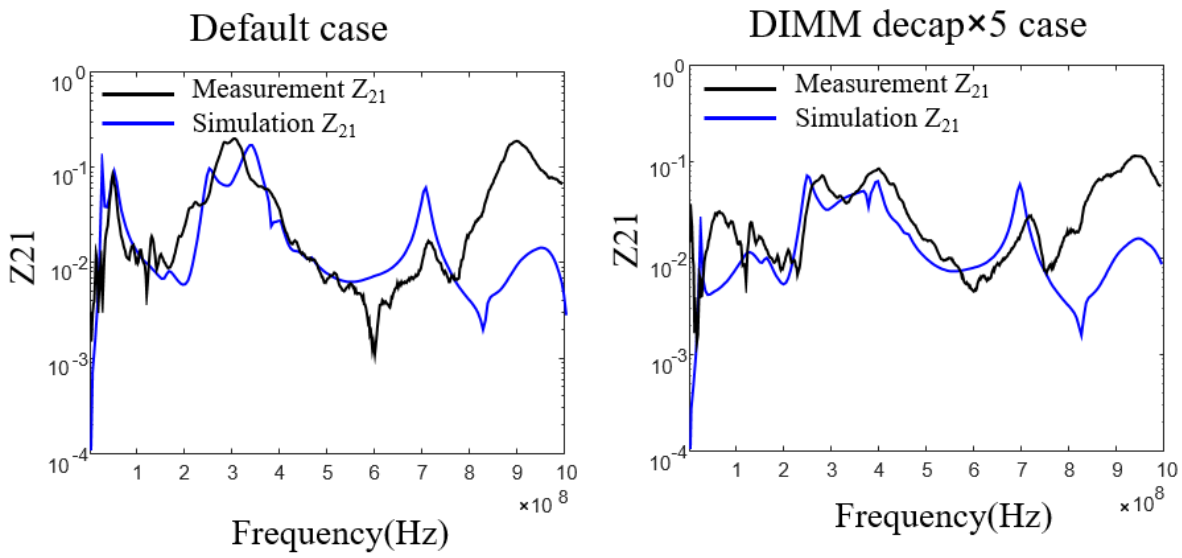


Fig. 11. HFSS Simulation Setup



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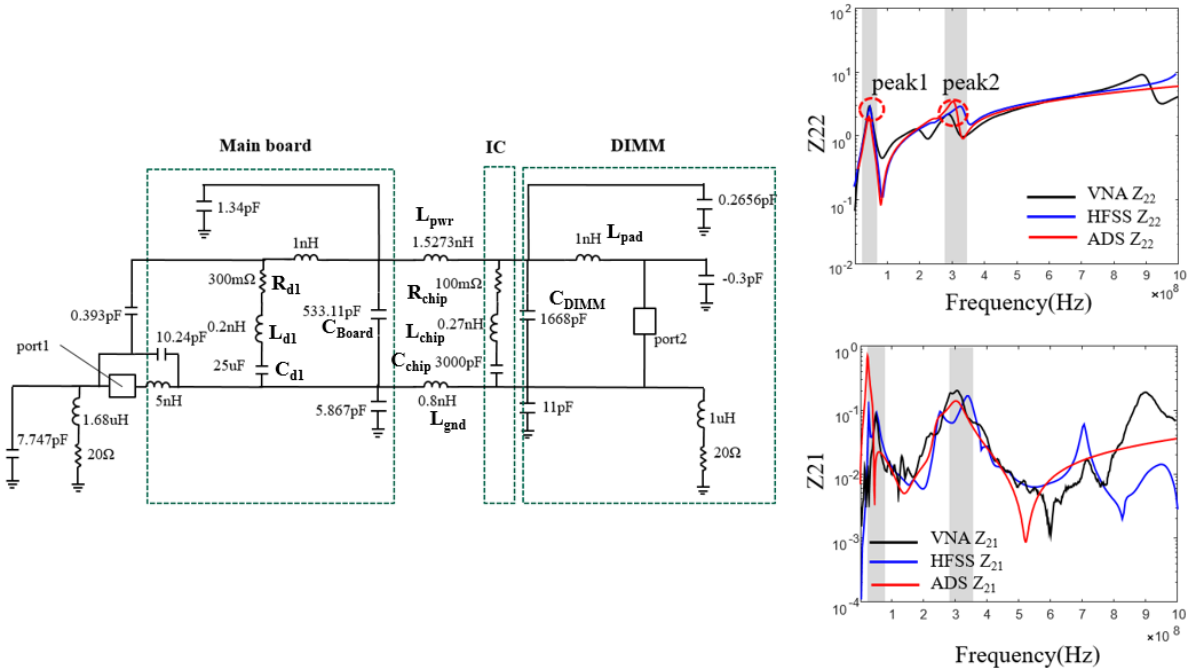

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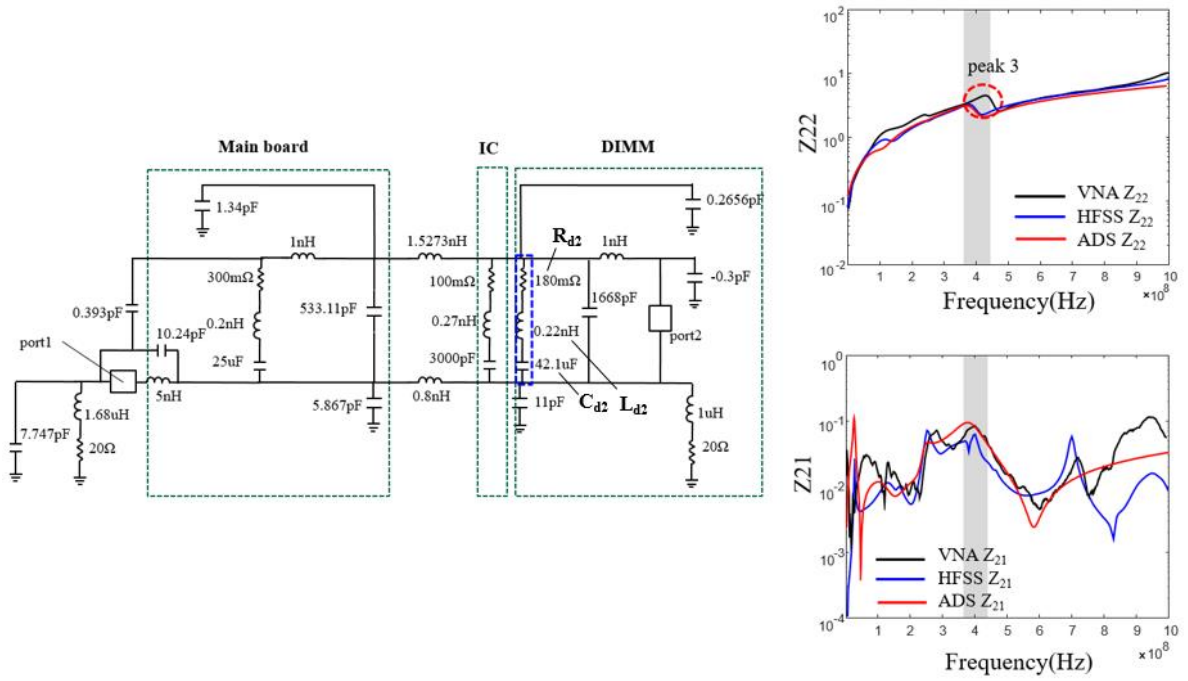


(c)

Fig. 12. (a) Comparison between Measured Z_{21} and HFSS Z_{21} (b) Circuit diagram of PCB & Z parameters of default case (case1) (c) Circuit diagram of PCB & Z parameters of DIMM de-cap×5 (case2)

Table 3

COMPONENT VALUES IN THE EQUIVALENT CIRCUIT

	C_{board}	C_{DIMM}	L_{pad}	R_{d1}	L_{d1}	C_{d1}	R_{chip}
Value	533.11pF	1668pF	1nH	300mΩ	0.2nH	25uF	60mΩ
	L_{chip}	C_{chip}	R_{d2}	L_{d2}	C_{d2}	L_{gnd}	L_{pwr}
Value	0.27nH	3000pF	180mΩ	0.22nH	42.1uF	0.8nH	1.5273nH

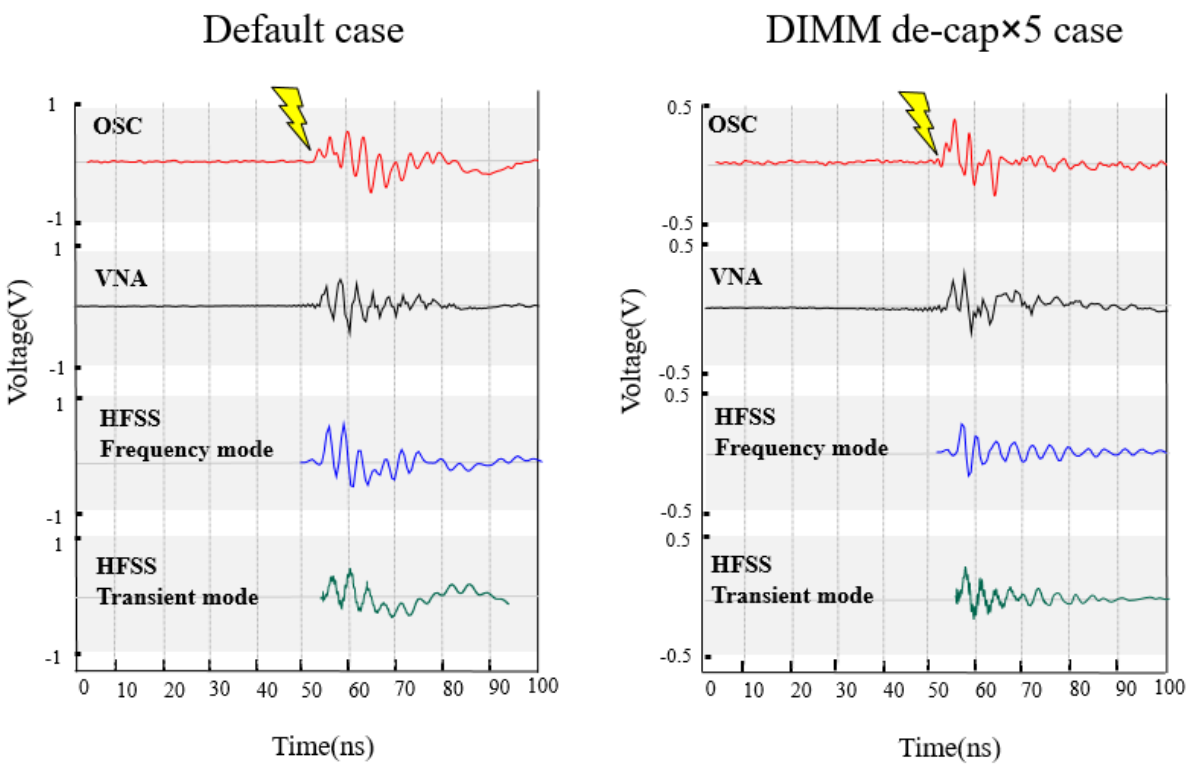
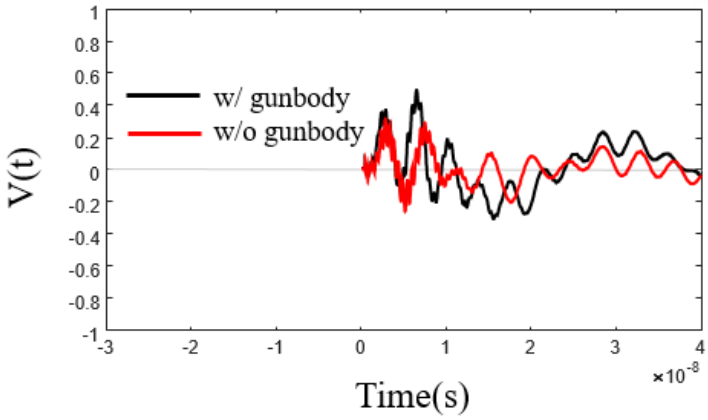
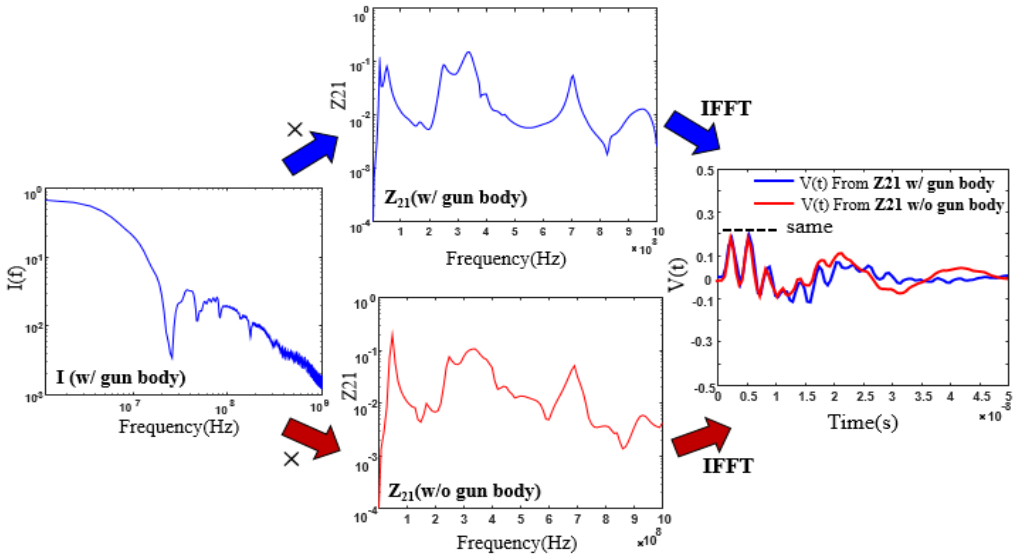


Fig. 13. Power-ground noise measurement, Measured Z_{21}×I, HFSS Simulation Z_{21}×I and HFSS transient mode



(a)



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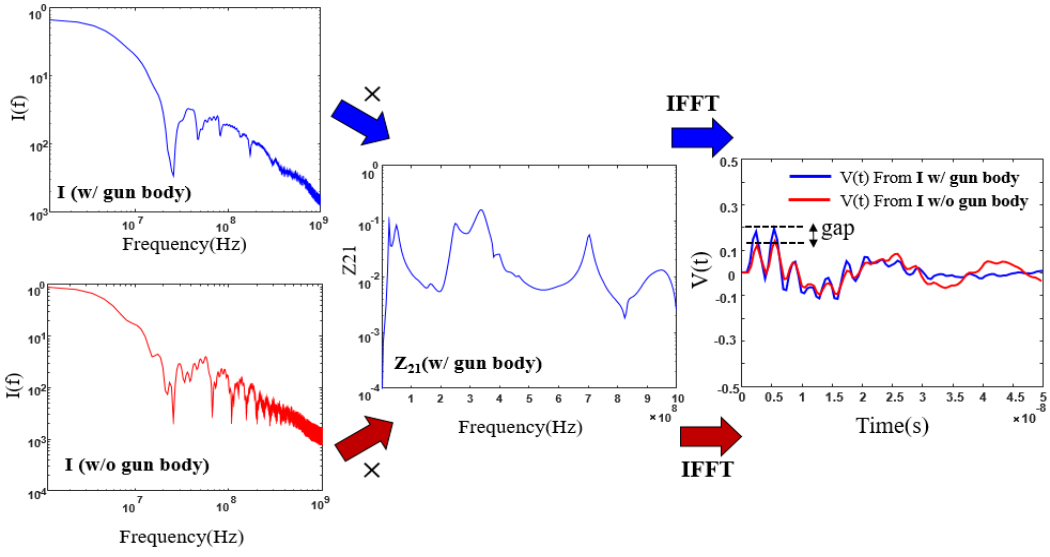
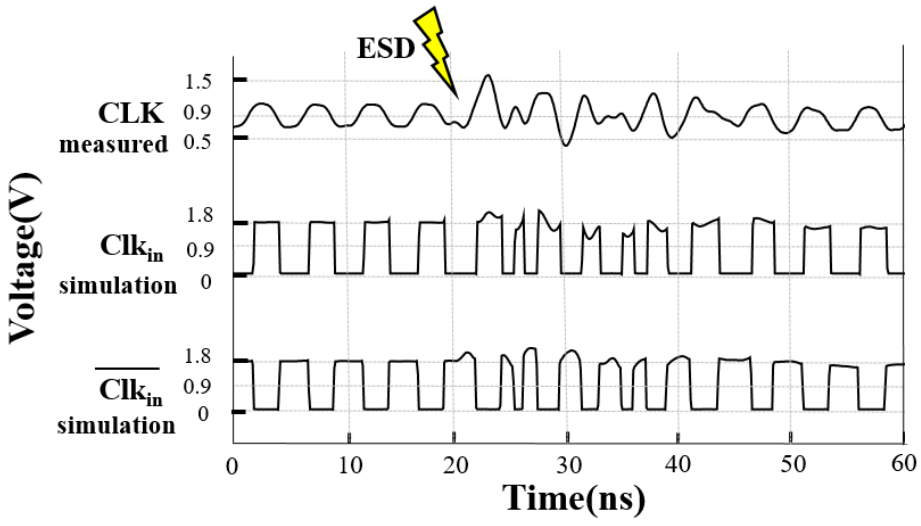


(c)

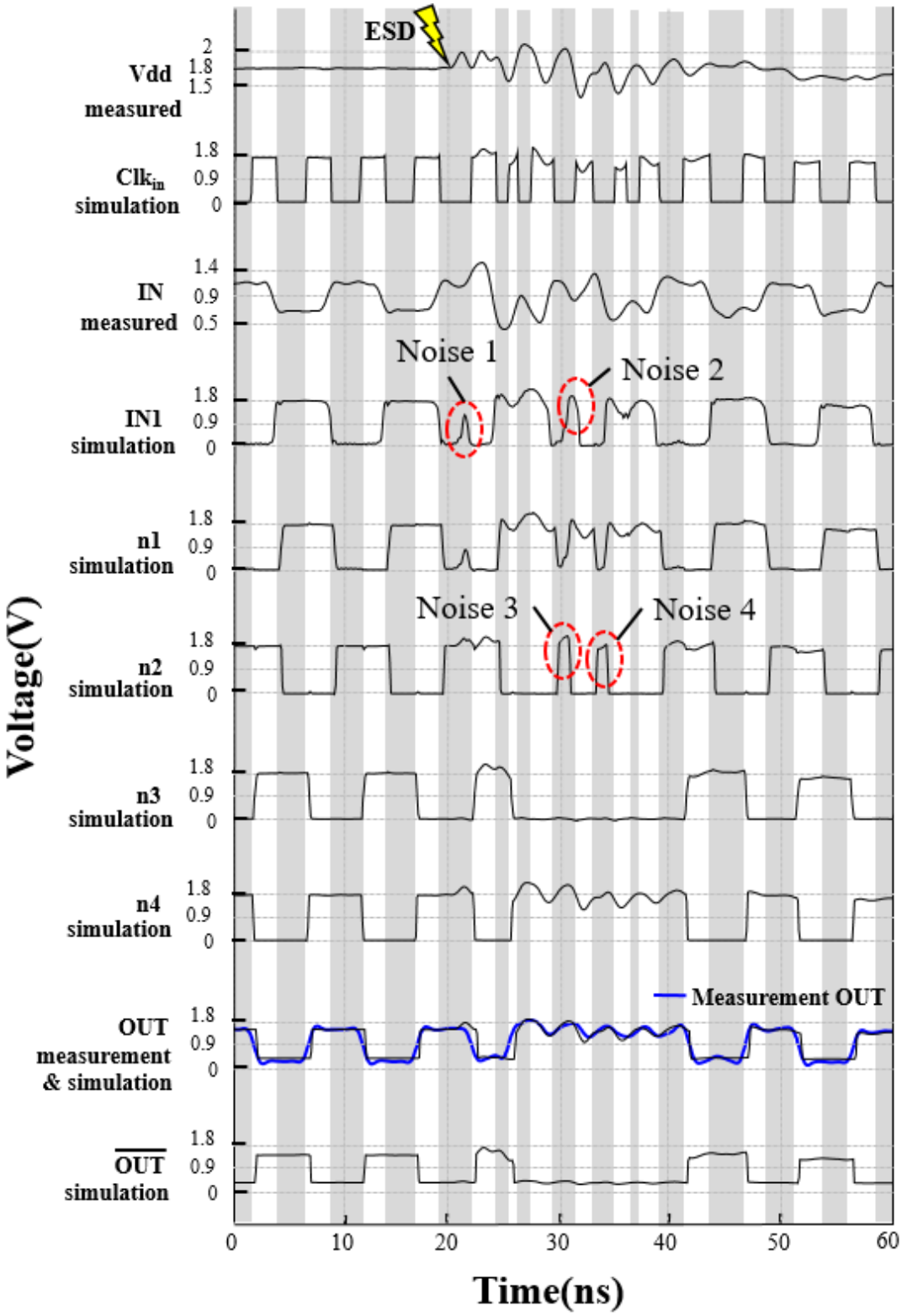
Fig. 14. Analysis of gun body effect on power-ground noise voltage (a) existence of gun body effect using HFSS Transient mode (5kV) (b) Calculation between input current w/ gun body and Z_{21} w/ gun body or w/o gun body (4kV) (c) Calculation between input current w/ gun body or w/o gun body and Z_{21} w/ gun body (4kV)

As shown in Fig.14 (a), It is confirmed that the existence of gun body has an effect on power-ground noise in HFSS transient simulation. To analyze the gun body effect to input current and main board, HFSS simulation tool is used in transient mode and frequency mode. Fig. 14 (b) shows that how does the existence of the gun body affect the Z_{21}. The input current and Z_{21} are obtained from HFSS transient mode and frequency mode, each and the excitation voltage is 4kV. At first, the input current with gun body multiplies by Z_{21} with gun body or Z_{21} without gun body, separately. And through the IFFT, the V(t) from Z_{21} with gun body and V(t) from Z_{21} without gun body are obtained. The first peaks of the noises are almost same. Therefore, the existence of the gun body has not a great effect on the Z_{21}. And Fig. 14 (c) shows that how does the existence of the gun body affect the input current. At first, the input current with gun body multiplies by Z_{21} with gun body. And, input current without gun body multiplies by Z_{21} with gun body. And through the IFFT, the V(t) from Input current with gun body and without gun body are obtained. The peak of first voltage between two cases is different. Therefore, we can draw a conclusion that the existence of the gun body has more effect on the input current than Z_{21}.

2.3 Verification of Measurement Results Using H-SPICE



(a)



(b)

Fig. 15. (a) Spice model logic timing chart of clock signals depending on ESD occurrence (b) Spice model logic timing chart of static F/F depending on ESD occurrence

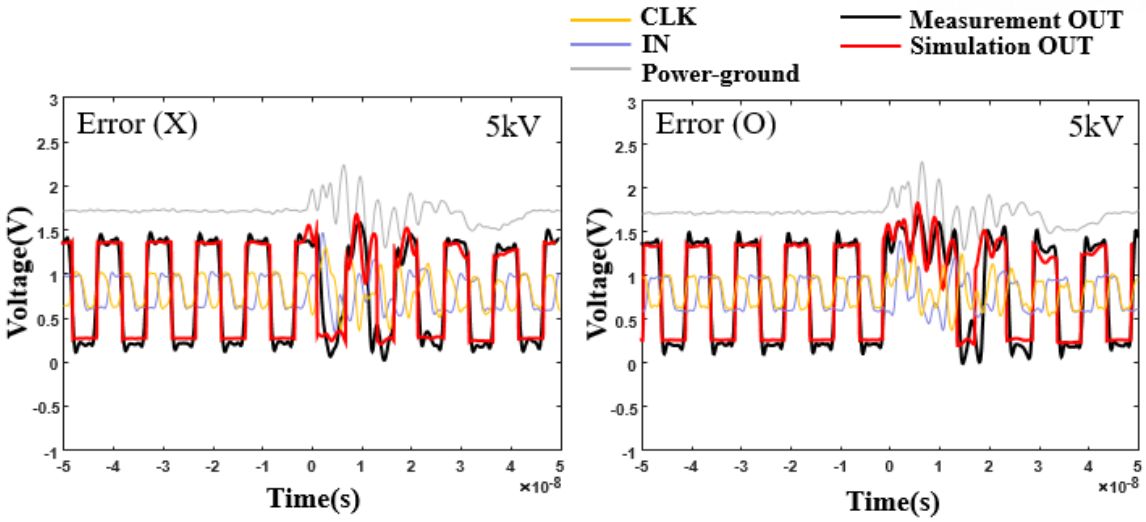
In order to verify the measured results and analyze the error in the circuit of the chip, power-ground noise, IN-ground noise and CLK-ground noise obtained from the experiment are applied to Vdd, IN and CLK of the simulation circuit respectively. From the H-spice simulation results, the signal form at each position of the circuit is analyzed. Fig. 6 (c) shows the static F/F circuit modeling for simulation. The CLK applied to the chip as a half swing is changed into a full swing through the clock buffer in chip, and each Clk_{in} and $\overline{Clk_{in}}$ is connected to T1 and T2. The timing chart of the CLK, Clk_{in} and $\overline{Clk_{in}}$ can be confirmed at Fig. 15 (a). CLK fluctuates after the 5kV ESD occurrence and changes to distinct signals after the buffer. Hence, the unexpected clock signal is additionally generated at Clk_{in} and $\overline{Clk_{in}}$. In other words, the number of rising and falling time are increased for about 20ns irregularly after ESD occurrence. Then, both the T1, which is open when clock signal is falling, and T2, which is open when clock signal is rising, are all affected.

The logic timing chart for CLK, IN and several positions of static F/F are shown in Fig. 15 (b). In common with CLK, the half-swing IN is also affected by fluctuation of the power-ground noise due to ESD. Considering both CLK and IN, it is confirmed that the signal tends to break already when a small swing enters the inverter.

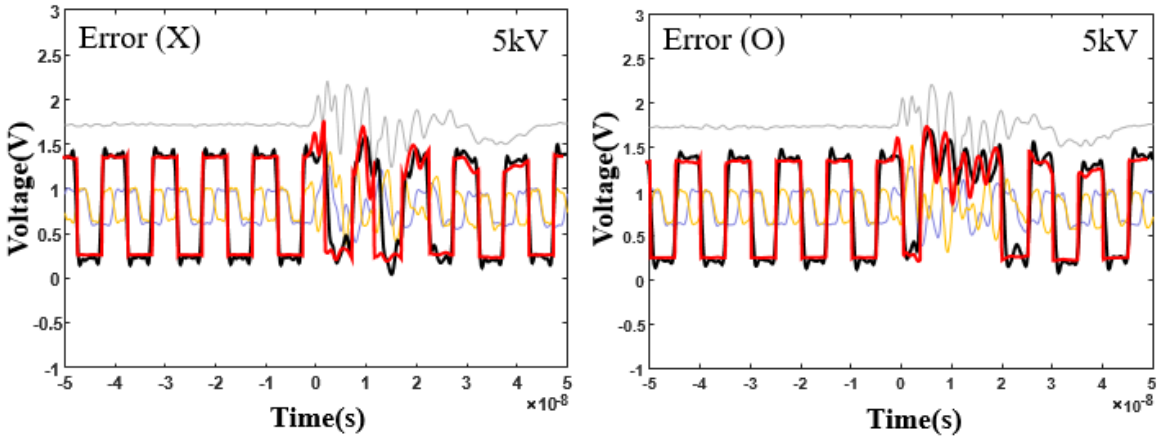
The Noise1 and Noise2 are confirmed at IN1. Because the Noise 1 disappears before the rising time of Clk_{in}, it is canceled. But the Noise 2 lasts until Clk_{in} changes to High and can be seen as a new signal at n1. On the other hand, both Noise 3 and Noise 4 are signals generated when T2 is closed, so they are not transmitted to n3 and disappear. n3 with temporary error goes n4 after the data store inverter and reaches the actual measurement point OUT through the buffer consisting of 4 inverters. The signals of the measurement OUT-ground noise and that of simulation OUT show good agreement.

Fig. 16 shows comparison between simulation and measurement OUT-ground noise based on simultaneous measured CLK-ground noise, IN-ground noise and power-ground noise under the three conditions. It can be confirmed that there are good correlations with high probability.

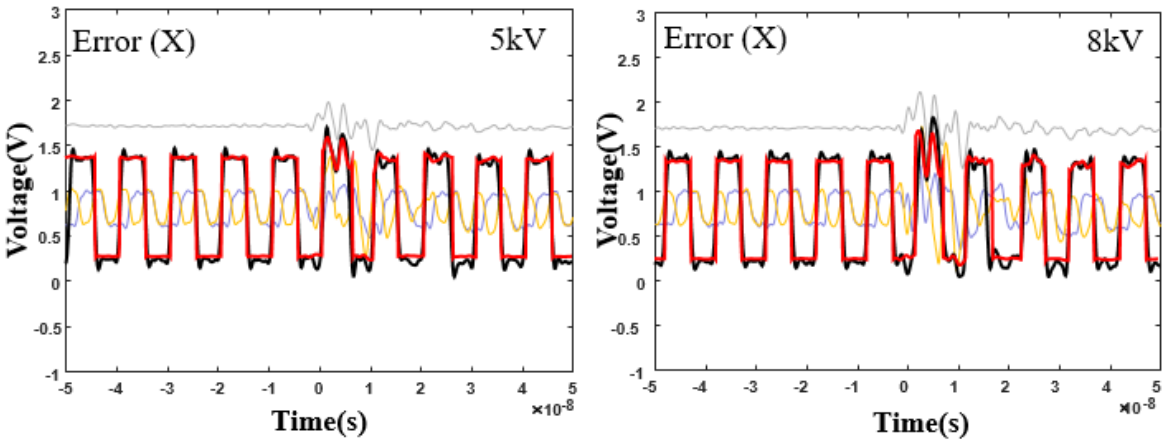
All measured IN-ground noise, CLK-ground noise and power-ground data are applied to Spice model to obtain error ratio of OUT signal in simulation. The OUT-ground error rates are compared between the measurements and simulations in Fig. 17. Each percentage represents the OUT-ground error rate in 50 experiments. At 5kV ESD occurrence, the reason for the difference in the error ratio depending on w/ or w/o of the chip shielding in the measurement is the direct coupling to wire-bond and IC die effect. Similar to the trend of measurement, in the simulation, it is confirmed that the error rate is significantly reduced when the DIMM de-caps exist.



(a)



(b)



(c)

Fig. 16. Comparison between noise voltage on PCB between measurement and simulation (a) case0 (b) case1 (c) case2

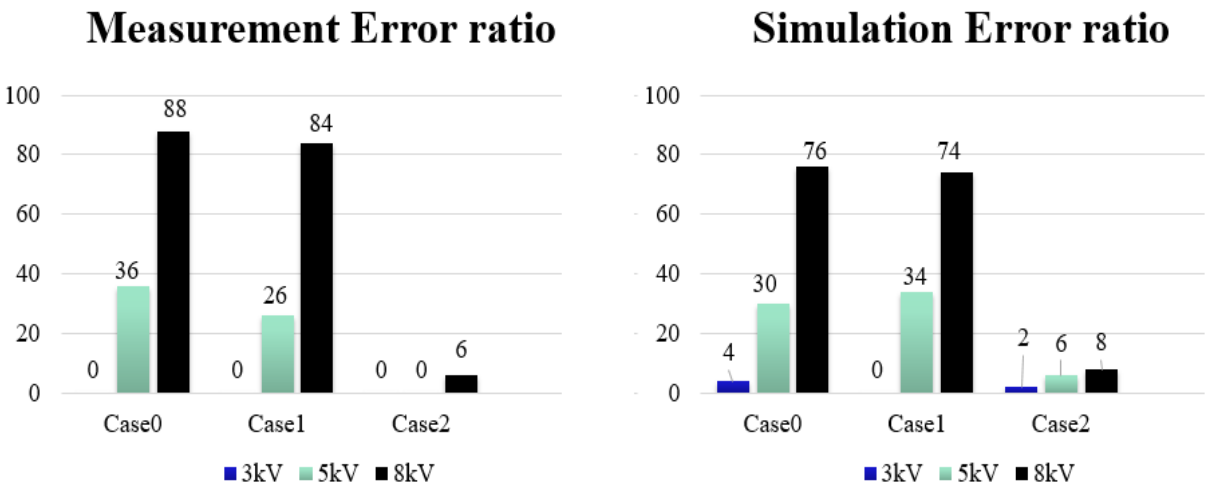


Fig. 17. Measurement and simulation temporary error ratio on PCB

2.4 Effective Number and Capacity of de-cap

2.4.1 Logic error ratio

Since the error tendency of the measurement results is obtained similar to the Spice simulation error tendency and the OUT form is identical, the measurement results can be relied upon. In order to find out how to reduce error in DIMM, efficient conditions for stable DIMMs are investigated by observing the error depending on the location and number of DIMM de-caps using this measurement method. Fig. 18 shows the location of the de-cap connected to the DIMM. a~c positions are close to the SODIMM socket and far away from the chip. Also, the d and e positions are close to both SODIMM socket and chip. All experiments are performed after connecting the chip shielding copper and three 10uF Board de-caps, the ESD level is 8kV.

The temporary error ratio depending on the number and capacity of DIMM de-cap in 50 times measurements is shown in Fig. 19. When DIMM de-cap is not connected, the temporary error rate is about 84%.

As can be seen from the error ratio, even if capacitors with large capacitances are used, the error is not greatly reduced when the number of connected capacitors is small. On the other hand, if capacitors

with a capacitance of 1.2nF or more are used, the error rate is greatly reduced when the capacitors are connected in distributed arrangement.

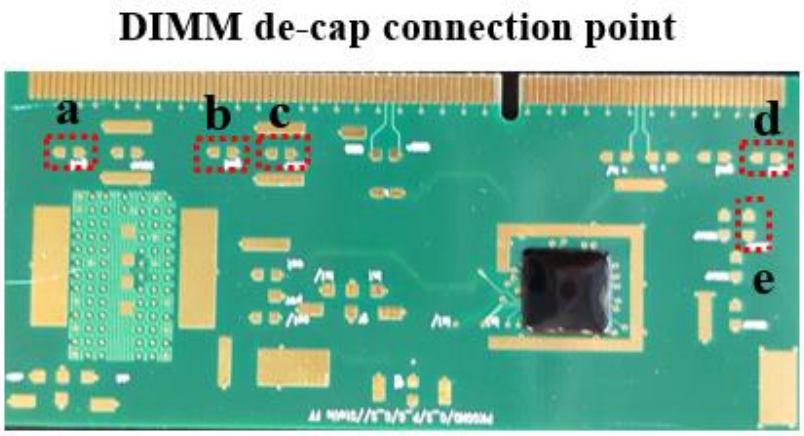


Fig. 18. Position of de-cap on DIMM

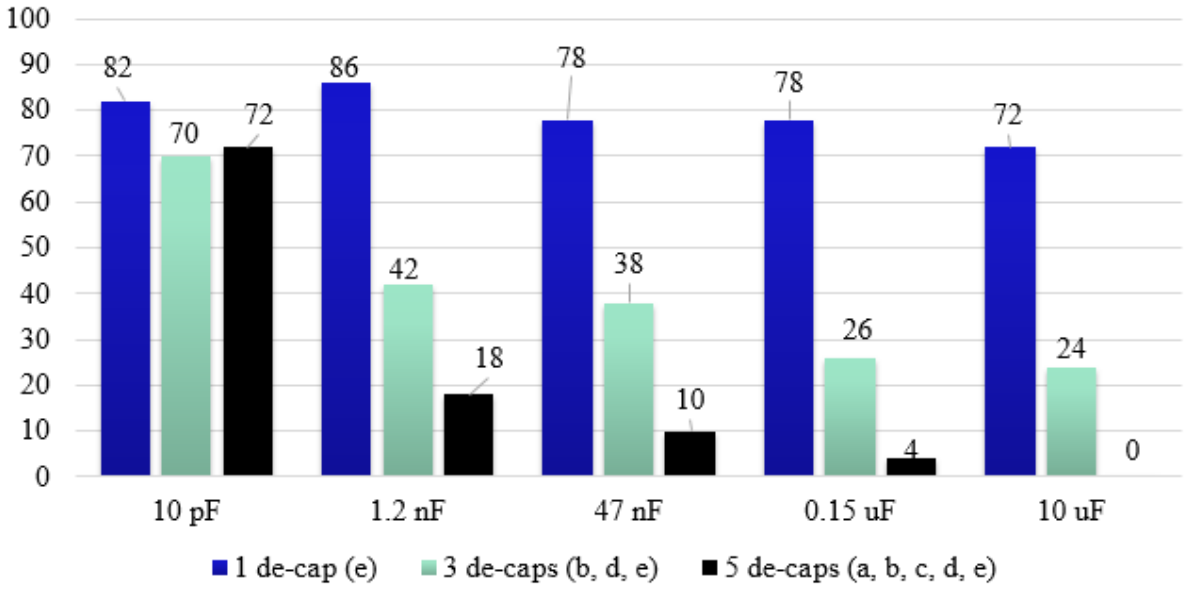
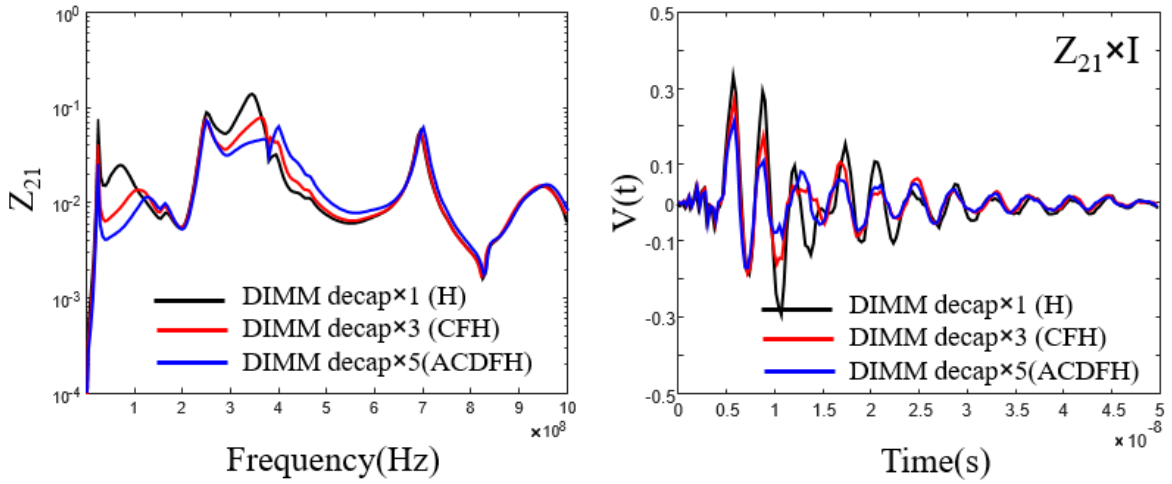
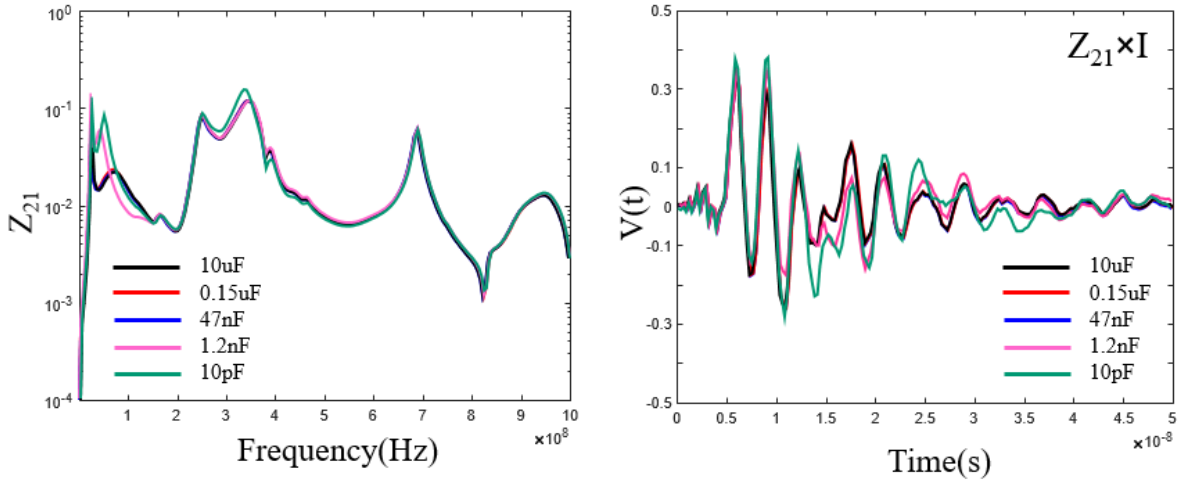


Fig. 19. Measurement error ratio depending on the number and capacity of de-cap

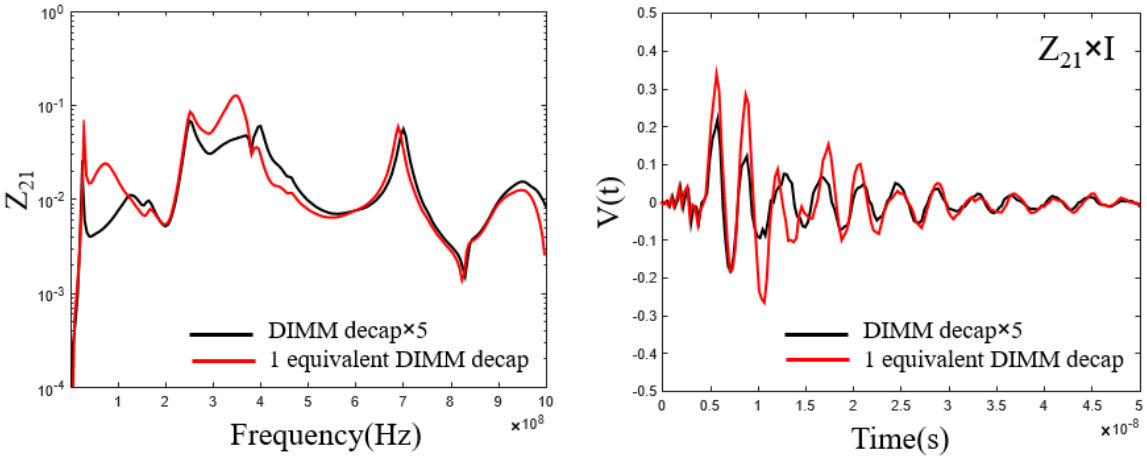
2.4.2 Analysis of de-cap effect using HFSS



(a)



(b)



(c)

Fig. 20. Z_{21} and $Z_{21\times}$I Using HFSS simulation (a) Tendency of the number of de-cap (b) Tendency of the capacity of de-cap (c) The effect of decentralized placement of de-cap

HFSS simulation tool is used to analyze the correlation between error ratio and power-ground noise fluctuation depending on the number and capacity of de-cap. The simulation setup is shown in Fig. 11, and the position of the de-cap is same as the actual connection point. The ESD occurrence level is 5kV. The power-ground noise fluctuation and Z_{21} results in simulation depending on the number of de-caps are shown in Fig. 20 (a). It can be seen that the Z_{21} peak of power-ground and $Z_{21}\times$I result also decreases. This result supports the fact that the error rate decreases when the number of de-caps are increased.

Also, Z_{21} and $Z_{21}\times$I results depending on de-cap capacity change are shown in the Fig. 20 (b). When a de-cap of 47nF or more is connected, it is confirmed that Z_{21} is obtained similarly, but for 1.2nF and 10pF, the first and second peak of Z_{21} increases. Therefore, the fluctuation of $Z_{21}\times$I value increase. Especially, the first peak and second peak of Z_{21} is increased drastically. If the de-cap C value is 1.2nF or less, de-cap does not play a role in maintaining the fluctuation between the power-ground of the DIMM. This result supports the fact that the error rate increases when de-cap is less than or equal to 1.2nF in Table IV.

Fig. 20 (c) shows how decentralized placement of de-cap is important when the total capacitances in two cases are same. It is confirmed that placing the capacitor at various location is effective in reducing power-ground noise.

III. Propose of Dynamic ESD Fields Measurements using the Probe-Factor Deconvolution

The soft failure due to the ESD events would be caused by either conducted noise coupling or radiated field coupling. The dynamic conducted noise voltages can be directly measured at decoupling capacitors or signal traces on printed circuit boards (PCBs) of the product, in section II. Meanwhile, the measurements of dynamic electromagnetic fields are also necessary for analysis of radiated field coupling due to the system-level ESD. In [5], the voltages measured in field probes are converted to the dynamic field quantities using compensation circuits and additional deconvolution process. Usually, the dynamic fields are obtained from the probe voltages using the probe-factor deconvolution process as a data post-processing. A straightforward method of probe-factor deconvolution process performs the following steps. 1) Perform the FFT of the voltage obtained by the field probe 2) Obtain the field in the frequency domain by multiplication of the probe factor and the voltage spectra. 3) Perform the IFFT of the field in the frequency domain to get the transient field quantity.

The conventional probe-factor deconvolution approach based on the FFT-IFFT has fundamental limitations due to the band-limited data and DC extrapolation of the probe-factor spectra, which may cause a causality and DC offset problems. In [16] and [17], the delay extraction and causality enforcement techniques for transient response waveforms have been introduced. By applying this approach, the dynamic E-field and H-field due to ESD events at a real operating laptop can be obtained without the causality or DC offset problems. This paper focuses on the probe-factor deconvolution process with the probe-factor delay explicitly enforced. The noise voltages induced at two lab-made probes for E- and H-Fields are converted to corresponding fields by calibrating the probe factor, which is extracted from measurements using GTEM cell and the vector network analyzer (VNA) [18]. Using the conventional and proposed methods, the E-field and H-field due to ESD occurrence at a real operating laptop are measured and compared.

3.1 Measurement Setup of the Noise Voltages Induced at Field Probes

In the ESD measurement setup, the electric field in both differential and common modes are captured

in the oscilloscope, since the oscilloscope is connected to the earth ground providing a common mode (CM) current path. The common mode current cannot be controlled and should be avoided. To prevent the voltage induced by common mode current, lots of ferrite cores are usually installed at the measurement cable, since the ferrite core provides the high impedance for the common mode current.

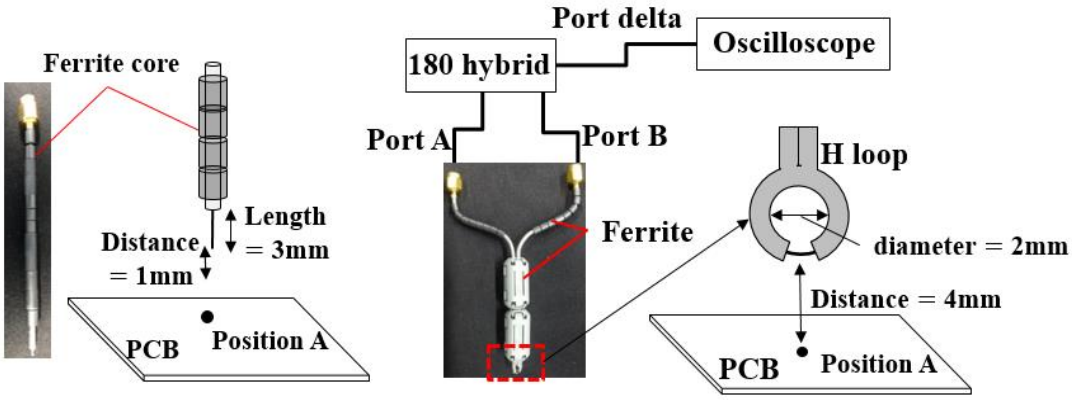


Fig. 21. The setup for the field measurement (a) The structure of the E-field probe and ferrite cores (b) H-field probe and measurement setup for the noise voltage induced at the probe

Fig. 21 (a) shows the measurement setup for the noise voltage induced at E-field probe at the position A. The E-field probe is simply made of a rigid cable, where the inner signal conductor is exposed by 3 mm. It is vertically located 1mm above the plane. An ESD event involves a high current with a fast rise time, also causing the magnetic field coupling on the signal traces. Fig. 21 (b) shows the measurement setup using the manufactured H-field probe. The outer grounds of two rigid cables are soldered each other to maintain the same reference potential. A loop with 2 mm diameter is then made by connecting two signal pins. The CM noise coupled at both pins is reduced using the ferrite cores, and further subtracted each other using a 180° hybrid coupler. Since the hybrid output voltage is attenuated by the hybrid gain of 0.63, the relation between the induced voltage and the measured voltage is given as $V_{meas} = V_{real} \times 0.63$. In the magnetic field measurement, the electric field also can be captured at the exposed loop. To block the E-field coupling in the H-field measurement, the signal pin is covered by the outer ground of the rigid cable as much as possible.

3.2 Probe-Factor Deconvolution Methods

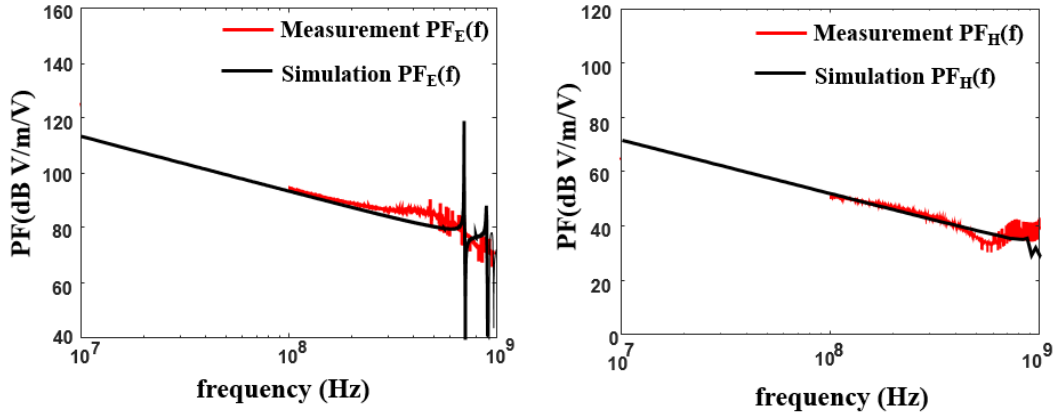
3.2.1 Proposed deconvolution process for field measurements

The ESD event is excited at the corner of the ground plane in the real laptop board. The ground plane is fluctuated up to a few hundred or thousand voltages in the ESD event, causing a strong electric field. The dynamic voltages measured in the E- and H-field probes should be converted to the field quantities. The calibration factor for conversion from the induced voltages to the field quantities can be extracted from the measurements using the VNA and the GTEM cell [6]. The port 1 is connected to the top port of the GTEM cell and the port 2 is connected to the probe installed on the side of the GTEM cell. The reference port for the phase measurement is port1. The E-field monopole probe is directly connected to the VNA, whereas the dual-rigid outputs of the H-field probe is connected through the 180˚ hybrid coupler. The probe factors can be extracted from the measured S-parameters as [18],

$$PF_E(f) = \frac{1}{S_{E,21}(f)\ d} = \frac{V_1^+(f)}{V_2^-(f)d} = \frac{E_{probe}^+(f)e^{j2\pi fT_d}}{V_2^-(f)} \quad (1)$$

$$PF_H(f) = \frac{1}{S_{H,21}(f)\ d\ \eta} = \frac{V_1^+(f)}{V_2^-(f)\ d\ \eta} = \frac{H_{probe}^+(f)e^{j2\pi fT_d}}{V_2^-(f)} \quad (2)$$

where the T_d represents the propagation delay from the port 1 to the probe position. The d is the distances from the septum to the outer ground of the GTEM cell. The $PF_E(f)$ and $PF_H(f)$ represent the probe factors of the E-field probe and H-field probe, respectively. The η is a wave impedance.



(a) (b)

Fig. 22. (a) Probe factor of E-field probe in frequency domain (b) Probe factor of the H-field probe including the 180° hybrid coupler in frequency domain

Fig. 22 shows the magnitudes of probe factors extracted from measurements and HFSS full-wave simulations using (1) and (2). Since the $S_{E,21}(f)$ and $S_{H,21}(f)$ include positive delays, the probe factors for the E-field probe and H-field probe include negative delays by the amounts. Therefore, the non-causal negative time delay in the probe factors are separately extracted and removed, before the probe factor in time-domain is calculated.

The probe factors of E-field probe and H-field probe can be decomposed as [17],

$$PF_E(f) = PF_{E,\min}(f) \cdot PF_{E,AP}(f) \tag{3}$$

$$PF_H(f) = PF_{H,\min}(f) \cdot PF_{H,AP}(f) \tag{4}$$

where the $PF_{E,min}(f)$ and $PF_{H,min}(f)$ are minimum phase functions with the negative delay removed, and the all-pass function with negative delay are specified as $PF_{E,AP}(f)$ and $PF_{H,AP}(f)$. The phase and the magnitude of the minimum phase function are related by the Hilbert transform as

$$\angle PF_{E \text{ or } H,\min}(f) = \frac{1}{\pi} \int_{-\infty}^{+\infty} \frac{\ln\left|PF_{E \text{ or } H}(f)\right|}{f - f'} df' \tag{5}$$

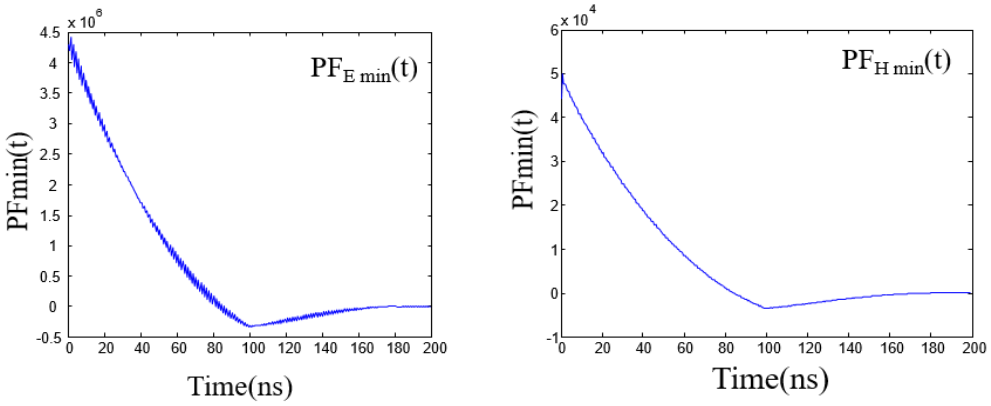
The negative time delay is then calculated as

$$T_d = \frac{\angle PF_{E \text{ or } H,AP}(f)}{2\pi f} \tag{6}$$

The transient field quantities are related to the transient induced voltage as convolution as

$$\begin{aligned} E \text{ or } H_{probe}(t) &= PF_{E \text{ or } H}(t) * v_{E \text{ or } H}(t) \\ &= PF_{E \text{ or } H,\min}(t + T_d) * v_{E \text{ or } H}(t) \end{aligned} \tag{7}$$

where the $V_E(t)$ and $V_H(t)$ are the transient measured probe voltages. $PF_{EorH,min}(t)$ represents the inverse Fourier transform of the minimum phase function of the probe factor. The negative time delay, T_d, can be separately enforced indicating that the field is actually generated prior to the induced voltages. The $PF_{EorH,min}(t)$ is denoted at Fig. 23.



(a) (b)

Fig. 23. Probe factor in time domain w/ minimum phase function (a) E-field probe factor (b) H-field probe factor

3.2.2 Validation of the Deconvolution Methods

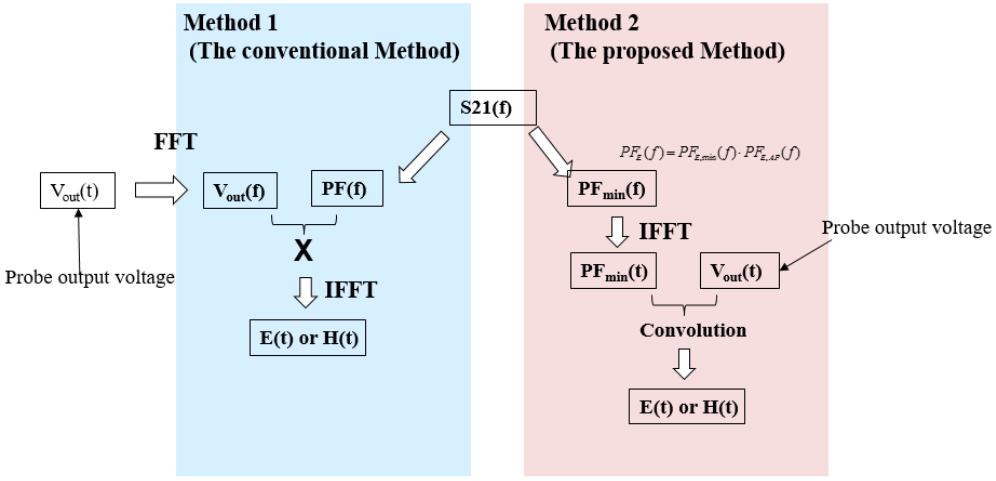


Fig. 24. The methods for obtaining the dynamic fields from noise voltage

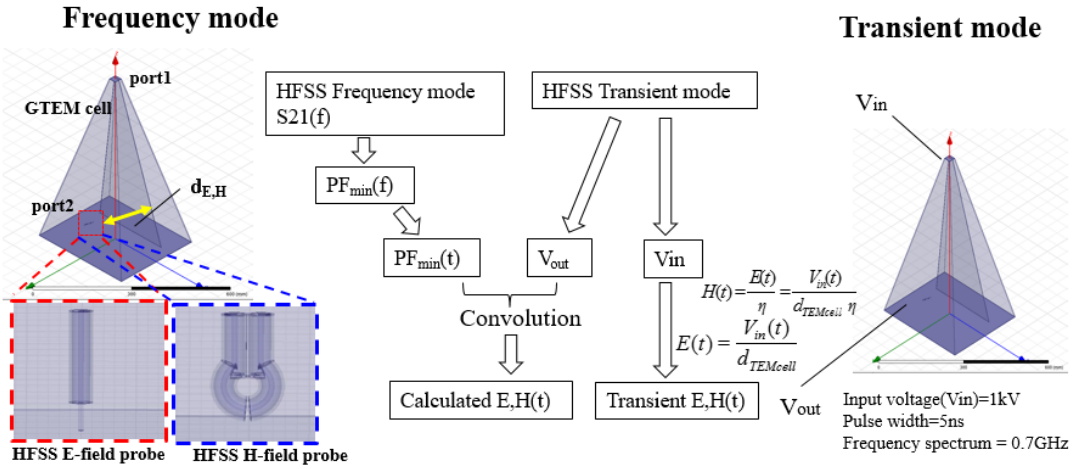
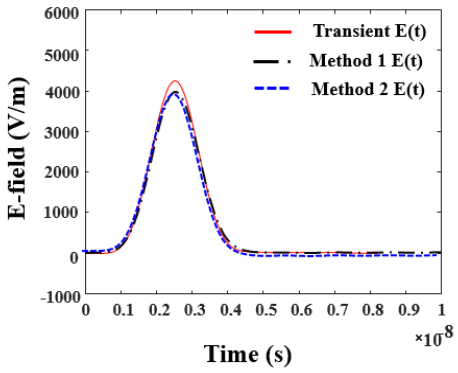
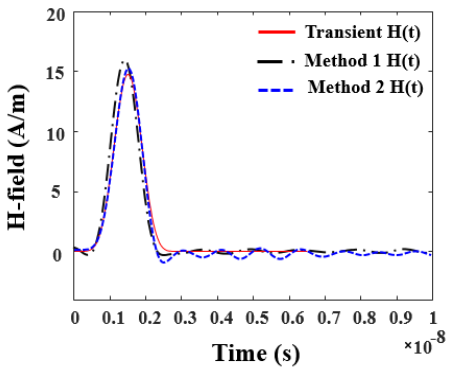


Fig. 25. Simulation setup for validation of the proposed PF deconvolution method



(a)

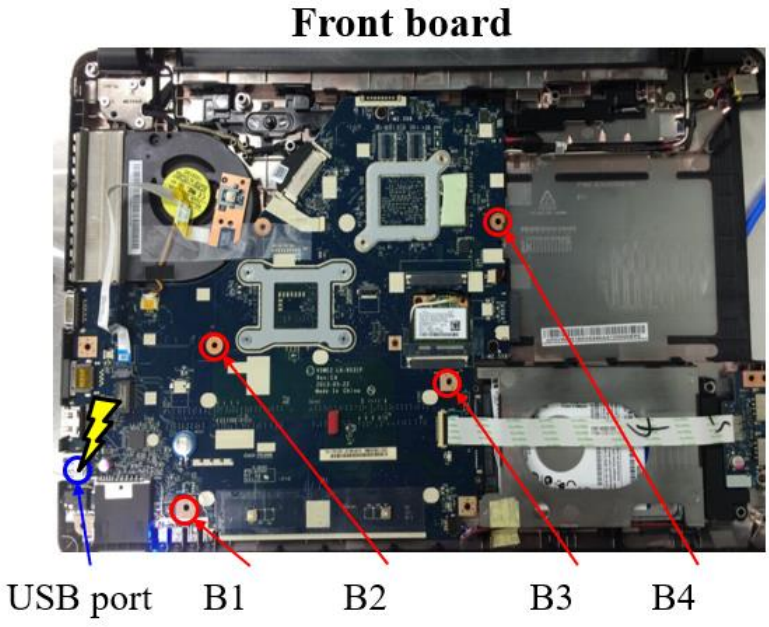


(b)

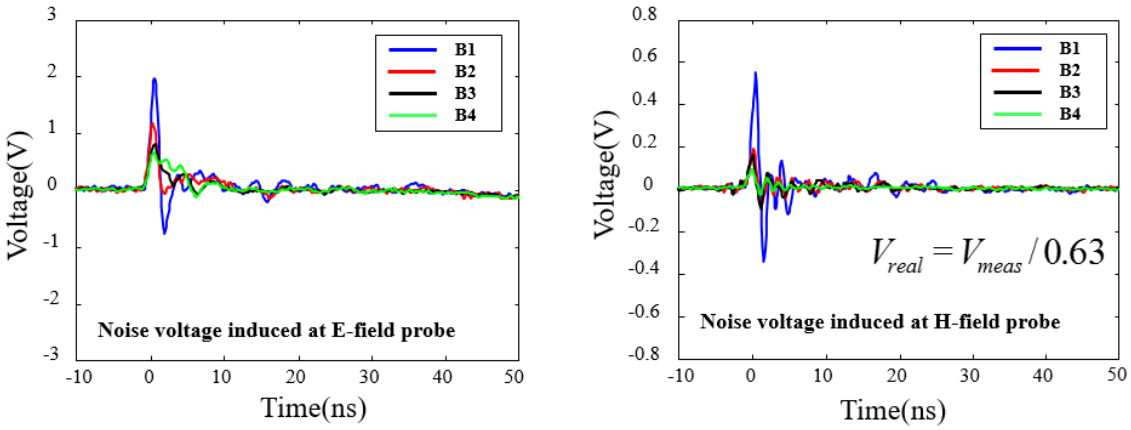
Fig. 26. Actual field and recovered fields by PF deconvolutions (a) E(t) (b) H(t)

The two deconvolutions methods (Fig. 24), 1): the conventional method based on IFFT of the product of PF(f) and V(f) (method1), 2): the convolution method with causality enforcement using (3)-(7), are validated in the HFSS transient solver simulations. As shown in Fig. 25, the simulation setup is similar to the GTEM cell simulation for the probe-factor extraction; the port 1 is connected to the top port of the GTEM cell and the port 2 is connected to the probe installed on the side of the GTEM cell. The input voltage at the GTEM cell port 1 is set as 1 kV Gaussian pulse with pulse width of 5 ns, and the dynamic fields at the location of probes as well as the probe voltages are observed at the same time. The specifications of the E-field probe and H-field probe in simulations are same as the actual ones used in measurements. In the method 2, the time domain probe factor with the delay removed is calculated by IFFT of $PF_{min}(f)$, which is obtained from additional HFSS simulations in frequency domain. The dynamic fields directly observed at the probe location are compared with the fields recovered from the probe voltages using the deconvolution methods (method1 and method2), as shown in Fig. 26 (a) and (b). It is shown that all results agree well for the case of Gaussian pulse field excitations.

3.3 Application to the Measurements of Dynamic ESD Fields



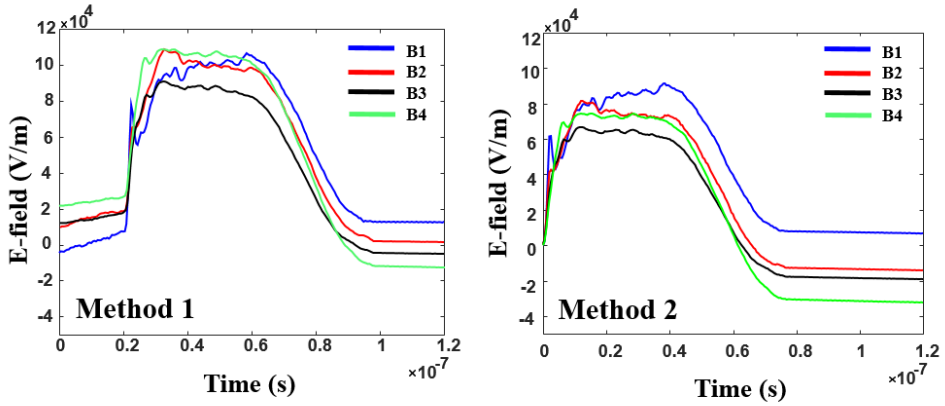
(a)



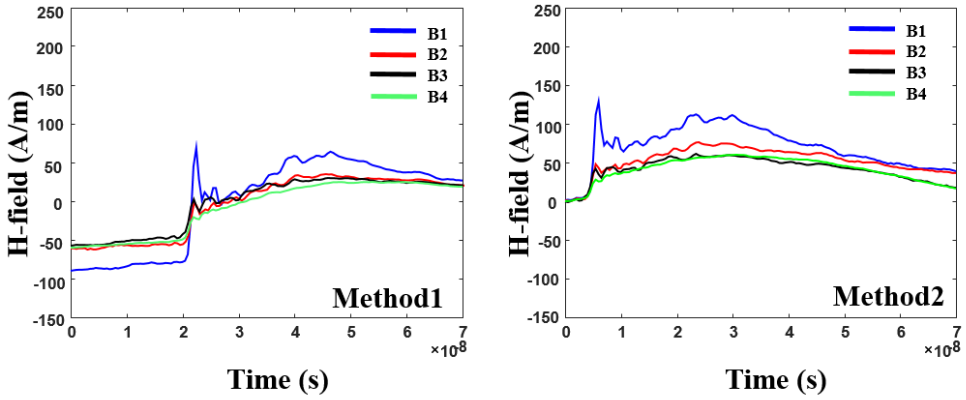
(b)

Fig. 27. (a) Measurement positions on the real operating laptop (b) Noise voltage induced at E- and H-field probe

Fig. 27 shows the measurement points on the real operating laptop and measured noise voltages at field probe. The voltages are measured with 4kV ESD events excited on the USB port. The measurement positions are B1, B2, B3 and B4. The induced voltage is significantly reduced as the measurement position is far from the ESD injection point. The waveforms of the field quantities obtained using the method1 and method2 are plotted in Fig. 28. In the case of method1, the DC offset significantly varies at different measurements. The DC extrapolation is necessary for the frequency domain PF(f), which may cause DC offset problem. Also, the starting point of the measured waveform is not clear in the method 1 because of the causality issue which is inherent from the band-limited frequency-domain data. However, in the case of method2, all the waveforms always start from the initial zero and there are no DC offset issues. Also, it is free from the causality problem, since the delay is explicitly enforced. As a numerical example, in Fig. 29, the probe factors were divided by 2 and the field waveforms were recovered. The method 2 provides the expected a half fields well, but the method 1 results in different DC offsets.

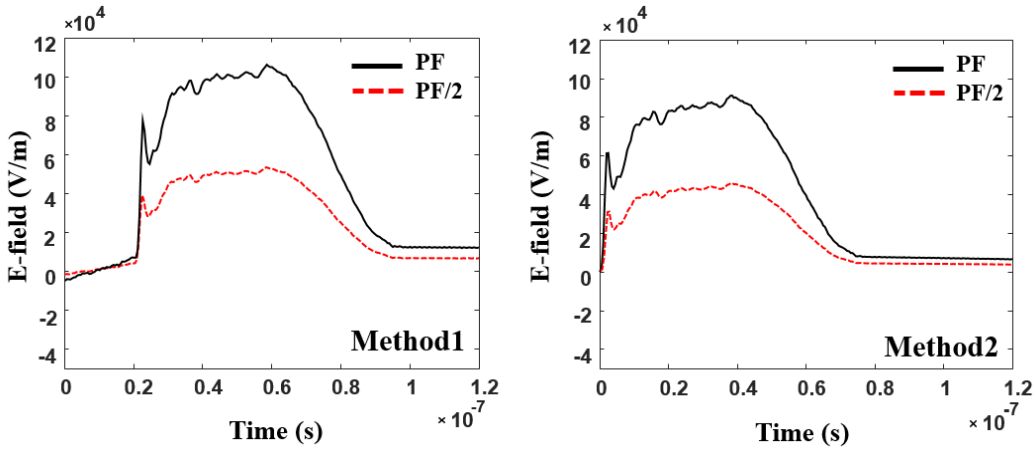


(a)

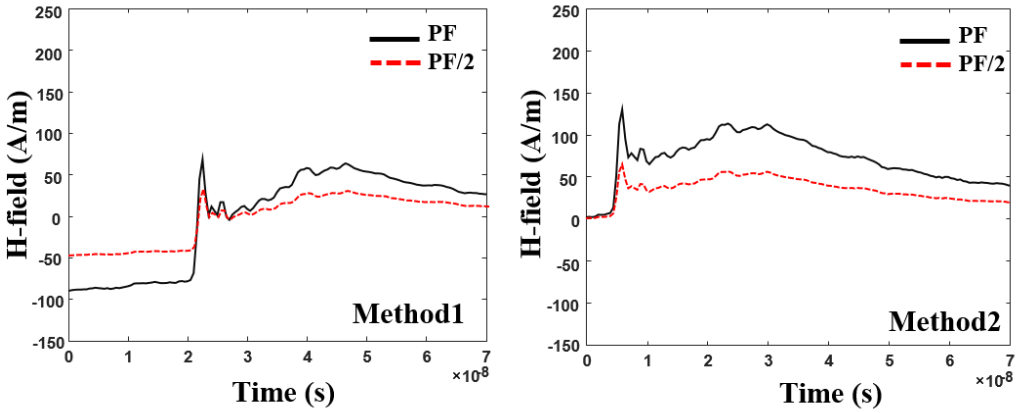


(b)

Fig. 28. Fields on the real operating laptop obtained using two deconvolution methods (a) E-field (b) H-field



(a)



(b)

Fig. 29. Fields obtained using different probe-factors at position B1 (a) E-field (b) H-field

IV. Summary and Conclusion

In this paper, basic F/F operation was confirmed by fabricating a simplified PCB based on real operating laptop. Based on the measurement of power-ground noise, IN-ground noise, CLK-ground noise and OUT-ground noise, analysis of error from chip due to ESD generation was performed. In addition, the error rate depending on existence of de-cap and chip shielding was investigated, and it is confirmed that the error is most drastically reduced in the presence of DIMM de-cap. Besides, error due to field coupling is also presents the error rate could be reduced by chip shielding.

Using the measurement method validated by Spice simulation, $Z_{21}\times I$ measurement technique and HFSS simulation, effective capacity and number of de-cap on DIMM are proposed to reduce error ratio and noises.

In section IV, a probe-factor deconvolution method for dynamic field measurements without the causality or DC offset problems is proposed. The E-field and H-field induced by ESD events at a real operating laptop are obtained using both the conventional and proposed deconvolution methods. In the application to the real product measurements, the conventional FFT-IFFT method shows the causality and DC offset problems due to the band-limited frequency-domain data and DC extrapolation, whereas the proposed methods are free from both causality and DC offset issues. The proposed probe-factor deconvolution method could allow more reliable and stable field measurements.

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Acknowledgement

석사과정 2년은 저에게 길고도 짧은 시간이었습니다. 그 기간 동안 저는 많은 분들로부터 조언과 도움을 받았습니다.

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IC-EMC Lab 구성원들에게도 감사 인사를 드립니다. 처음 랩에 들어왔을 때 상담 해주고, 랩 생활에 잘 적응하게 도와준 랩장 동일이, 연구 노하우와 논문 쓰는데 큰 도움을 받은 준식이에게 감사합니다. 그리고 자기일처럼 같이 연구하고 고민해준 상영이, 경진이에게도 감사하다는 말을 전하고 싶습니다. 앞으로 연구실을 빛내게 될 명조와 우룡이도 여러가지로 도와주어서 감사합니다.

항상 저를 위해 기도하시고 믿어 주시는 사랑하는 부모님과 인생의 멘토이자 멘티인 동생들에게 감사드립니다. 건강하시고 주님 안에서 언제나 행복한 우리 가정이 되길 기도하겠습니다. 또한 석사 생활을 가까이서 지켜보며 힘이 되어 준, 앞으로의 모든 시간을 함께할 진화에게도 감사하다는 말을 전합니다.

사랑하는 가족들에게 저의 조그마한 열매인 이 논문을 바칩니다.